

S2000 Single-Chip Microcomputer Family

AMI's S2000 family of single-chip microcomputers offers a wide range of capability to the user seeking flexible, adaptable system(s) at low cost. The S2000 family provides the ideal solution to appliance and industrial/process-control applications. With versatile keyboard-oriented inputs, and outputs which can drive either LED or fluorescent displays directly, the S2000 family is designed specifically to minimize system parts count and cost.

Table I. S2000 Family Features

	S2000	S2150	S2200	S2400
ROM (x8)	1K	1.5K	2K	4K
RAM (x4)	64	80	128	128
Interrupts	—	—	3	3
A/D CONV (8 Channel)	—	—	8-Bit	8-Bit
Counter/Timer	+50/+60	+50/+60	8-Bit	8-Bit
Max Subroutine Levels	3	3	5	5
Instructions	51	51	59	59
Cycle Time (μ s)	4.5	4.5	4.5	4.5
High Voltage (Fluorescent Display Drive Version)	S2000A	S2150A	S2200A	S2400A

The S2000 family provides the advantages of computer architecture to low cost, minimum-parts-count display keyboard oriented control systems.

S2000/2150 Features

- 1024 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2000
- 1536 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2150
- 64 x 4 Scratchpad RAM On Chip — S2000
- 80 x 4 Scratchpad RAM On-Chip — S2150
- 13 Outputs and Inputs, Plus 8 Bi-Directional Three-State Lines
- Touch Control™ Capacitive Touchplate Interface
- Seconds Timer for Both 60Hz and 50Hz Lines
- 7-Segment Decoder and LED Display Drivers On Chip
- Single 9.0 Volt Supply
- Fast 4.5 μ s Execution Cycle
- Three-Level Subroutine Stack
- TTL-Compatible Outputs
- Reset, Test, and Single Step Modes
- Access to All Internal Registers and Memory for Debug and Test
- Crystal Input for Accurate Clocking — S2150
- Low Power RAM Retention, 20 μ A/Bit Typ @ 4V — S2150

S2000A/2150A Vacuum Fluorescent Display

The S2000A/2150A are identical to the S2000/2150 but provide high voltage fluorescent display capability. The output buffer drive (V_{DD}) is changed to a vacuum fluorescent drive (V_{FD}) and typically tied to 32 volts. The D_0 through D_7 and A_0 through A_4 are changed from LED drivers (nominal 5 volts) to vacuum fluorescent drivers (nominal 26 volts).

S2200/2400 Features

The S2200/2400 provide a quantum jump in chip features beyond the S2000. In addition to all the features the S2000 offers, the S2200 gives the added flexibility of interrupts and the sophistication of an on-chip A/D or D/A converter capable of multiplexing 8 channels of analog data making it suitable for a wide range of applications.

- 2048 x 8 Program ROM On Chip Expandable to 8192 x 8 — S2200
- 4096 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2400
- 128 x 4 Scratchpad RAM On Chip
- RAM Save Power Down Mode (Mask Option)
- Two-Level Interrupt Stack
- System with Provision for Software Interrupt
- Programmable 8-Bit Timer/Event Counter On Chip
- 13 Outputs, 9 Inputs, Plus 8 Bi-Directional Three-State Lines
- Touch Control™ Capacitive Switch Interface
- 7-Segment Display Decoders and LED Drivers
- TTL-Compatible Outputs
- Single +9V Power Supply
- 4.5 μ s Cycle Time
- 59 Instructions — 52 Single Byte and Single Cycle
- 3-Level Subroutine Stack
- 2-Level Interrupt Stack
- Built-In Production Test Mode
- Single-Step Capability
- Power-Fail Detect, RAM Keep-Alive and Power-On Reset Circuitry
- 8-Bit A/D Converter (Up to 8 Channels)
- D/A Converter Capability (Mask Option)
- Up to 256 General Purpose Flags
- 6 Special Flags
- Table Look-Up Capability
- S2200A/2400A Vacuum Fluorescent Display Capability

S2000 Family

	S2000	S2000A	S2150	S2150A	S2200	S2200A	S2400	S2400A
Product Characteristics								
ROM (Bytes)	1K	1K	1.5K	1.5K	2K	2K	4K	4K
RAM (Nibbles)	64	64	80	80	128	128	128	128
A/D Converter (8-Bit)	—	—	—	—	YES	YES	YES	YES
Timer	50/60Hz	50/60Hz	50/60Hz	50/60Hz	PROG 8BIT	PROG 8BIT	PROG 8BIT	PROG 8BIT
Interrupts	—	—	—	—	3	3	3	3
Power Fail Detect	—	—	—	—	YES	YES	YES	YES
High Voltage Outputs	—	YES	—	YES	—	YES	—	YES
Crystal Clock Option	—	—	YES	YES	YES	YES	YES	YES
TouchControl Inputs	YES	YES	YES	YES	YES	YES	YES	YES
Levels of Subroutine	3	3	3	3	5	5	5	5
# of Flags	2	2	2	2	262	262	262	262
Power-Down RAM Option	—	—	YES	YES	YES	YES	YES	YES
D/A Converter Option	—	—	—	—	YES	YES	YES	YES
Zero — Crossing Detect	YES	YES	YES	YES	YES	YES	YES	YES
Cycle Time (μsec)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Instructions — Total	51	51	51	51	59	59	59	59
Single Cycle & Byte	49	49	49	49	52	52	52	52

Development Support

Microcomputer Development Center	YES	YES	YES	YES	YES	YES	YES	YES
Logic Analyzer	YES	YES	YES	YES	YES	YES	YES	YES
Hardware Emulator	#2150	#2150A	#2150	#2150A	#2400	#2400A	#2400	#2400A

S2000 Family Support

The S2000 single-chip microcomputer family, unlike many microprocessors, does not leave the designer or industrial OEM unsupported. The S2000 Family features a proven array of development aids:

Microcomputer Development Center (MDC) — AMI's MDC is a fully equipped, dual-floppy disk-based microcomputer development facility, complete with FDOS-II Floppy-Disk-Operating and File Management System. Controlled from its CRT terminal, MDC provides instant access to program and data files resident on removable diskettes.

Development Software — The MDC's software includes self-diagnostics and a comprehensive Text Editor and PROM programmer package that support S2000 software development. In addition, S2000 software includes a MACRO Assembler, Loader, and Instruction Simulator.

Cross-Assemblers editor and simulator debug — Available on a major timesharing service.

Logic Analyzer — The MDC-140 Logic Analyzer is an advanced debug tool connected as a peripheral device of the AMI Microcomputer Development Center (MDC). Features include:

- Captures 1024 Events of 40 Parallel Inputs
- Captures Data Under Control of Programmable Start on Data Content
- Delay of -1024 to +64K Clock Periods
- Setup and Display of Captured Data Under Control of MDC Software
- Display Format is User-Definable; Captured Data Can Be Displayed in a Mix of Hex, Octal, Binary, ASCII and Special Formats for Support of S6800, S6820, S2000, 8080, etc.
- Four Clock Sources
- Input Voltage Range = -15 to +15 volts
- Adjustable Input Thresholds
- Data-Dependent Output for Triggering an Oscilloscope

SES-2150(A)/SES-2400(A) — The SES-2150/2400 Emulator boards are pin-for-pin substitutes for S2000 microcomputer family chips. The Emulator Boards use conventional UV erasable PROMs for program storage.

In addition, a specialized module is used to provide emulation of the S2150A/S2400A high voltage vacuum fluorescent display drivers.

Customer Assistance — AMI's S2000 Family Applications Engineering Staff is readily available for consultation regarding any aspects of S2000 Family usage. The AMI staff is also available to discuss any special modifications to the S2000 for high volume applications.

S2000 Family Instruction Set Summary

The S2000 and S2150 contain 51 instructions, all single byte, with 49 that are single cycle. The S2200 and S2400 contain 59 instructions, of which 52 are single cycle and single byte.

Nearly all S2000/2150 instructions are common to the entire family, which allows the programmer to develop software expertise and easily move up the S2000 product line.

Register Instructions

S2000/2150	S2200/2400	
LAI X	LAI X	X → ACC, 0 ≤ X ≤ 15; (In S2000/2150 Select I and K Inputs also)
LAB	LAB	BL → ACC
LAE	LAE	E → ACC
XAB	XAB	BL → ACC
XABU	XABU	BU → ACC, (IN S2150, BITS 2, 1, AND 0; IN OTHERS, BITS 1 AND 0 ONLY)
XAE	XAE	ACC → E
LBE Y	LBE Y	Y → BU, E → BL, 0 ≤ Y ≤ 3
LBZ Y	LBZ Y	Y → BU, 0 → BL, 0 ≤ Y ≤ 3
LBF Y		Y → BU, 15 → BL, 0 ≤ Y ≤ 3
LBEP Y		Y → BU, E + 1 → BL, 0 ≤ Y ≤ 3
	SRB	1 → BA
	RRB	0 → BA
	LMDI X +	X(6) → BA, X(5 - 4) → BU, X(3 - 0) → BL
	RAR	ACC(I) → ACC(I - 1), ACC(0) → CARRY, CARRY → ACC(3)
	XAK	KSR → ACC
	LANG	ACC → AR(3 - 0), RAM → AR(7 - 4)
	LNMA	ACC → NR(3 - 0), RAM → NR(7 - 4), THEN NR → BIN
	MOD	ACC → MOD(3 - 0), RAM → MOD(7 - 4)
	RBIN	BIN(3 - 0) → ACC; BIN(7 - 4) → RAM

RAM Instructions

S2000/2150	S2200/2400	
LAM Y*	LAM Y*	RAM → ACC, BU ⊕ Y → BU
XC Y*	XC Y*	RAM → ACC, BU ⊕ Y → BU
XCI Y*	XCI Y*	ACC → RAM, BL + 1 → BL, BU ⊕ Y → BU SKIP IF BL = 0 (AFTER INCREMENT)
XCD Y*	XCD Y*	ACC → RAM, BL - 1 → BL, BU ⊕ Y → BU SKIP IF BL = 0 (BEFORE DECREMENT)
STM Z	STM Z	1 → RAM BIT Z, 0 ≤ Z ≤ 3
RSM Z	RSM Z	0 → RAM BIT Z, 0 ≤ Z ≤ 3
	LMA	ACC → RAM
	STMI Z +	1 → RAM BIT Z, 0 ≤ Z ≤ 255, (RAM BANK 1)
	RSMI Z +	0 → RAM BIT Z, 0 ≤ Z ≤ 255, (RAM BANK 1)

Input/Output Instructions

S2000/2150	S2200/2400	
INP	IND	D3-D0 → ACC, D7-D4 → RAM
OUT	OUT	ACC → D3-D0, RAM → D7-D4 (NOT LATCHED)
DISN	DISN	ACC → SEGMENT DECODER → DISPLAY LATCH → D6-D0, CARRY → DISPLAY LATCH → D7
DISB	DISB	ACC → DISPLAY LATCH → D3-D0, RAM → DISPLAY LATCH → D7-D4
MVS	MVS	A-LINE MASTER STROBE LATCH → A LINES
PSH	PSH	PRESET HIGH [BL] → MASTER STROBE LATCH
PSL	PSL	PRESET LOW [BL] → MASTER STROBE LATCH
EUR		(EUROPEAN) SET 50/60Hz AND DISPLAY LATCH POLARITY
	INK	K3-K0 → ACC, K7-K4 → RAM

* + 8 bits in the second byte of an instruction.

* Assembled code contains complement of those arguments (the assembler does it automatically).

S2000/S2150 and S2200/S2400 Instruction Set Summary

Program Control Instructions

S2000/2150	S2200/2400	
PP X*	PP X*	IF PREVIOUS INSTRUCTION = PP, X-PPR ($0 \leq X \leq 15$)
JMP X	JMP X	IF PREVIOUS INSTRUCTION = PP, X-PBR ($0 \leq X \leq 7$)
JMS X	JMS X	JUMP TO LOCATION X, X-LR ($0 \leq X \leq 15$)
RT	RT	EXCEPT IF PREVIOUS INSTRUCTION = PP
RTS	RTS	JUMP TO SUBROUTINE AT X, LR+1-L STACK, PR-P STACK,
NOP	NOP	X-LR, 15-PR EXCEPT IF PREVIOUS INSTRUCTION = PP
	RTI	L STACK-LR, P STACK-PR
	TLU	L STACK-LR, P STACK-PR, SKIP INSTR.
		NO OPERATION
		RETURN FROM INTERRUPT, RESTORE REGISTERS
		IF PREVIOUS INSTRUCTION WAS A PP, DO A TABLE LOOK-UP
		SEQUENCE:
		PC+1-STACK
		RAM-PC(3-0), ACC-PC(7-4), PPR(3-2)-PC(9-8)
		ROM(7-4)-RAM, ROM(3-0)-ACC
		STACK-PC.
		IF PREVIOUS INSTRUCTION WAS NOT A PP, DO AN INDEXED
		SUBROUTINE CALL:
		PC+1-STACK
		RAM-PC(3-0), ACC-PC(7-4)

Skip Instructions (Skip 1 Non-PP Instruction) (RAM = Memory at BU,BL)

S2000/2150	S2200/2400	
SZC	SZC	SKIP IF CARRY = 0
SZM Z	SZM Z	SKIP IF RAM BIT Z = 0, $0 \leq Z \leq 3$
SZK	SZK	SKIP IF K BIT(S) = 0, (BIT(S) IN LAST LAI)
SBE	SBE	SKIP IF BL = E
SAM	SAM	SKIP IF ACC = RAM
SZI		SKIP IF I BIT(S) = 0, (BIT(S) IN LAST LAI)
SOS		SKIP IF SF = 1, 0-SF. (SF = 'SECONDS' FLAG OUTPUT OF +50/+60 COUNTER)
TF1		SKIP IF FLAG 1 = 1
TF2		SKIP IF FLAG 2 = 1
	SZMI Z +	SKIP IF RAM BIT = 0, (IN RAM BANK 1) $0 \leq Z \leq 255$
	SKFL X +	SKIP IF FLAG = 1

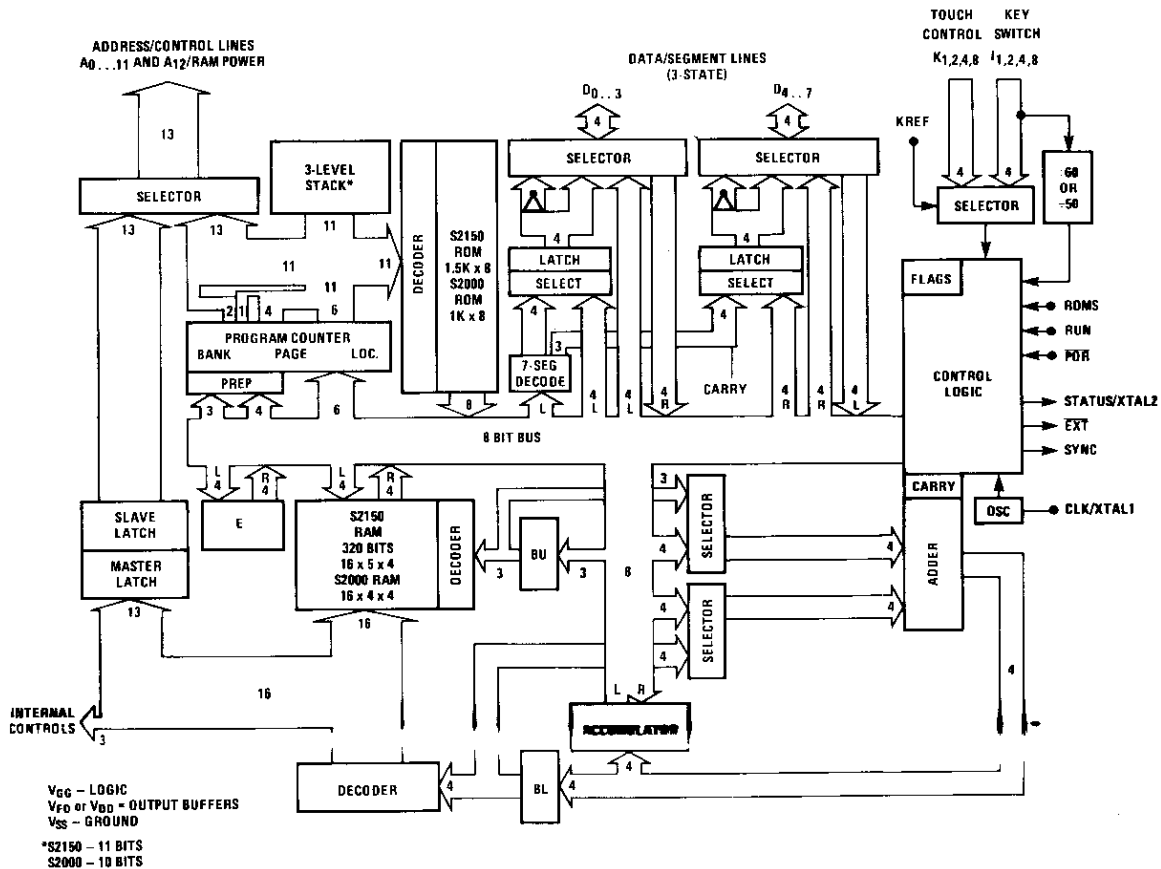
Arithmetic and Logical Instructions

S2000/2150	S2200/2400	
ADCS	ADCS	RAM + ACC + CARRY - ACC + C, SKIP IF SUM ≤ 15
ADIS X	ADIS X	X + ACC - ACC, SKIP IF SUM ≤ 15 , CARRY UNALTERED
ADD	ADD	ACC + RAM - ACC, CARRY UNALTERED
AND	AND	ACC & RAM - ACC
XOR	XOR	ACC \oplus RAM - ACC
STC	STC	1-CARRY
RSC	RSC	0-CARRY
CMA	CMA	15 - ACC - ACC (LOGICAL 1's COMPLEMENT ACC)
SF1		1-FLAG 1
RF1		0-FLAG 1
SF2		1-FLAG 2
RF2		0-FLAG 2
	SFLG X +	1-FLAG X
	RFLG X +	0-FLAG X

+ 8 bits in the second byte of an instruction.

*Assembled code contains complement of those arguments (assembler does it for you).

AMI S2000/2150 Detailed Block Diagram



S2000/S2150 Pin Configuration

(GRD) V _{SS}	1	40	D ₃
D ₂	2	39	D ₄
D ₁	3	38	D ₅
D ₀	4	37	D ₆
ROMS	5	36	D ₇
EXT	6	35	SYNC
(P.C. MSB) A ₁₂	7	34	RUN
A ₁₁	8	33	K ₈
A ₁₀	9	32	K ₄
A ₉	10	31	K ₂
A ₈	11	30	K ₁
V _{DD} /V _{FD}	12	29	V _{GG} (+9V)
A ₇	13	28	I ₈ AND TIMER
A ₆	14	27	I ₄
A ₅	15	26	I ₂
A ₄	16	25	I ₁
A ₃	17	24	K _{REF} TOUCH CONTROL
A ₂	18	23	CLK*
A ₁	19	22	POR
(P.C. LSB) A ₀	20	21	STATUS*

*May be used for crystal input on S2150/2150A

Pin Descriptions — S2000/2150

PIN NO.	NAME	DESCRIPTION
1	V _{SS}	Most negative power-supply input. Typically grounded.
29	V _{GG}	Most positive power-supply input. Typically +9V.
12	V _{DD} (S2000) V _{FD} (S2000A)	Power supply input for all output buffers. Typically tied to V _{GG} or to a +5V supply. Power supply input for HV drive. Typically +32V
4 - 2, 40 - 36	D0 - D7	D Lines for input and output. Output during instructions OUT, DISN, DISB. Input during INP. Float at reset time or after an MVS instruction; or if RUN pin is low; or after a PSL with BL = 14. Display Latch outputs (DISN, DISB) can be inverted using EUR.
20 - 13 11 - 7	A0 - A12	A Lines for addressing and control. Changed by MVS as set up by PSH/PSL. When external program ROM is used, these lines output the contents of the Program Counter during the first half of each instruction cycle.
5	ROMS	ROM source control. Tied to a logic 1 or 0 to indicate internal ROM only, or internal plus external. Tied to SYNC to override Bank 0 with an external program, and to inverted SYNC to verify internal ROM contents.
6	$\overline{\text{EXT}}$	Active-low strobe output for D Lines. Generated by an OUT instruction during time T7.*
35	SYNC	Synchronization output for external devices or for external ROM control. Continuous square wave, low in T1 and T3, high in T5 and T7.* $f_{\text{CLK}} + f_{\text{SYNC}} = 4$ for S2000, 8 for S2150.
34	RUN	Run/Wait control for prototyping and single-step testing. Logic 1 to run, logic 0 to wait with D Lines floating.
22	$\overline{\text{POR}}$	Power-On-Reset. Needs only an external capacitor, typically .05 microfarad. A pull-up to V _{GG} (15 μ A nominal) is provided internally.
23	CLK	On-chip oscillator connection. Runs at ~850kHz when connected to V _{SS} through 47pf and to V _{GG} through 30k Ω on the S2000. Crystal control possible; consult AMI.
21	STATUS	Monitors internal status for special designs. Logic 1 vs. logic 0 indicates: (during T1)* D Lines floating or not floating; (T3) BL equal or not equal to 13 for multiplex control; (T5) Carry is 1 or 0; (T7) Next instruction will or won't be skipped. On the S2150 a mask option allows use as a crystal oscillator pin.
24	KREF	K Lines voltage comparator reference input. Typically +3.0V, supplied by an external resistor divider.
30 - 33	K1, K2 K4, K8	K Lines, tested by SZK instruction. Any combination of these lines, selected by the last executed LAI instruction, are gated into the signal input of the voltage comparator. Unselected K Lines are discharged to V _{SS} , at 160 μ A typical.
25 - 28	I1, I2, I4, I8	I Lines, with internal pull-ups of 100 μ A nominal. Any combination of these lines, selected by the last executed LAI instruction (S2000, S2150), are gated into a common node tested by the SZI instruction. I8 also clocks a seconds timer whose output is tested using SOS.

*T1 is the first quarter-cycle following the falling edge of the SYNC output, T3 is the second, T5 is the third, and T7 is the fourth.

S2000/2150

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Operating Temperature (special request)	-40°C to +85°C
Maximum Positive Voltage	+18V
Maximum Negative Voltage	-0.3V
Maximum Output Currents	(See "Conditions" below)
I_{DD} Supply Current (depends on output loads)	+75mA
Total Average Power Dissipation	+700mW

S2000/2150

Electrical Characteristics

($V_{SS} = 0V$, $V_{GG} = +7.5V$ to $+10.0V$, $V_{DD} = 5V^*$, $T_A = 0^\circ C$ to $+70^\circ C$, $f_{SYNC} = 125kHz$ to $225kHz$)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_1 thru K_8					$2.8 < K_{REF} < 3.2V$
	Low Level	0		$K_{REF} - 0.5$	V	
	High Level	$K_{REF} + 0.5$		V_{GG}	V	
INPUTS	I_1 thru I_8 , POR					(Note 1)
	Schmitt-trigger					
	Low Level	0		1.7	V	
	High Level	5.3		V_{GG}	V	
INPUTS	ROMs, RUN					
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level - Program	5.0		V_{GG}	V	
	High Level - Data	3.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.8	V	$I = +25mA^{**}$
OUTPUTS	A_4 thru A_{12}					
	\overline{EXT} , SYNC, & S					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.6	V	$I = +5mA^{**}$
OUTPUTS	D_0 thru D_7					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		1.0	V	$I = +12mA^{**}$
I_{GG}	Supply Current		28	50	mA	
Δ RAM	RAM "Keep Alive"		20		$\mu A/Bit$	$V_{RAM} = 4.0V$
			30		$\mu A/Bit$	$V_{RAM} = 9.0V$

NOTE 1: There is an internal pull-up of $100\mu A$ nominal ($15\mu A$ nominal on \overline{POR}) from each of these inputs to V_{GG} .

* V_{DD} may be connected to V_{GG} if single power supply operation is desired.

**At $V_{GG} \geq 8.5VDC$

Δ Available only on S2150/S2150A.

S2000A/S2150A

Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Operating Temperature (special request)	- 40°C to + 85°C
Maximum Positive Voltage, V_{FD} , A_0 - A_4 , D_0 - D_7	+ 33V
All other pins	+ 18V
Maximum Negative Voltage, any pin	- 0.3V
Maximum Output Currents	(See Conditions below)
Source Current, any pin	- 10mA
Total Average Power Dissipation	+ 700mW
Rate of Rise of V_{FD}	1.6V/msec.
Maximum Voltage at V_{FD} with respect to V_{GG}	+ 22V

S2000A/S2150A

Electrical Characteristics — Specifications noted only for parameters which change from the S2000/2150 to the S2000A/2150A.

($V_{SS} = 0V$, $V_{GG} = 7.5$ to $10.0V$, $V_{FD} = V_{GG} + 22V$, $T_A = 0^\circ C$ to $+ 70^\circ C$. $f_{SYNC} = 125kHz$ to $225kHz$)

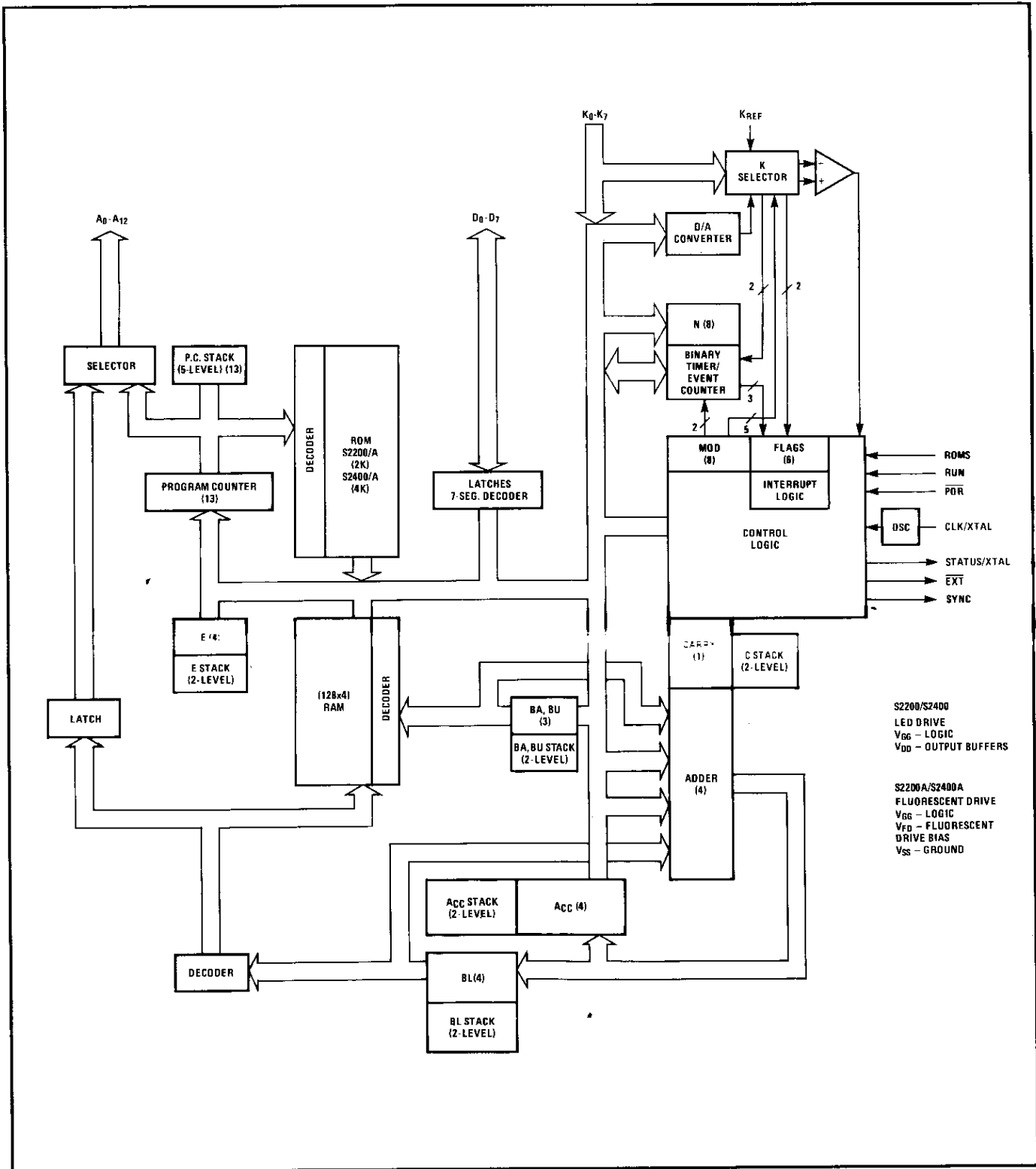
	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7 , A_0 thru A_4					
	High Level	- 3.5			mA	$V_{OUT} = V_{FD} - 6V^{**}$ $I = 250\mu A^{**}$
	Low Level			0.6	V	
OUTPUTS	A_5 thru A_{12} , EXT. SYNC. & STATUS					
	High Level	3.5			V	$I = - 5mA^{**}$
	Low Level			0.6	V	$I = + 5mA^{**}$
I_{GG}	Supply Current		28	50	mA	No Loads

NOTE 1: The output buffers for lines A_5 - A_{12} are supplied from V_{GG} .

NOTE 2: The high voltage parts, when biased with normal V_{FD} , are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

**At $V_{GG} \geq 8.5VDC$



S2200/2400 Block Diagram

For applications such as pulse width measurement, interval timing and event counting, the S2200/2400 has an 8-bit binary down-counter which counts 256 distinct states. The number of states (1 to 256) is controlled by the (Modulo-) N Register.

Another register, the MOD Register, controls the selection of inputs and outputs for the Programmable Counter/Timer, as well as the Display Latch output polarity and the voltage comparator's noninverting-input source.

S2200/2400 Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Operating Temperature (special request)	-40°C to +85°C
Maximum Positive Voltage	+18V
Maximum Negative Voltage	-0.3V
Maximum Output Currents	(See Conditions p. 12)
I_{DD} Supply Current (depends upon output loads)	+75mA
Total Maximum Power Dissipation	+700mW

Electrical Characteristics

($V_{SS} = 0V$, $V_{GG} = +7.5V$ to $+10.0V$; $V_{DD} = +5V^*$, $T_A = 0^\circ C$ to $+70^\circ C$, $f_{SYNC} = 125kHz$ to $225kHz$)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_0 thru K_7				V	For Touch-Control and Keypress Inputs
	Low Level	0		$K_{REF} - 0.5$	V	
	High Level	$K_{REF} + 0.5$		V_{GG}	V	
INPUT	K_{REF}	0		$2/3 V_{GG}$	V	
INPUTS	K_0 thru K_7				V	For A/D Conversion As Logic Inputs
	For A/D Conversion	0		$2/3 V_{GG}$	V	
	Logic Low Level			0.8	V	
	Logic High Level	3.5			V	
INPUT	POR					
	Low Level (POR Reset)	0		1.0	V	
	High Level	$1/2 V_{GG}$		V_{GG}	V	
	Power Fail			V_{GG}	V	
	- No Interrupt				V	
	- Interrupt	$V_{GG} + 1$			V	
INPUTS	ROMs, RUN					(Note 1)
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level	4.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.8	V	$I = +25mA^{**}$
OUTPUTS	A_4 thru A_{12}					
	EXT, SYNC, & S					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		0.6	V	$I = +5mA^{**}$
OUTPUTS	D_0 thru D_7					
	High Level	3.5		$*V_{DD}$	V	$I = -5mA^{**}$
	Low Level	0		1.0	V	$I = +12mA^{**}$
I_{GG}	Supply Current		28	50	mA	
I_{RAM}	RAM "Keep Alive" Current		20		$\mu A/Bit$	$V_{RAM} = 4.0V$

* V_{DD} may be connected to V_{GG} if single power supply operation is desired.

**At $V_{GG} \geq 8.5VDC$

Note 1: There is an internal pullup of 100 μA nominal from each of these inputs to V_{GG} .

S2200A/S2400A Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Operating Temperature (special request)	-40°C to +85°C
Maximum Positive Voltage, V_{FD} , A_0 - A_4 , D_0 - D_7	+33V
All other pins	+18V
Maximum Negative Voltage	-0.3V
Maximum Output Currents	(See Conditions below)
Source Current, any pin	-10mA
Total Average Power Dissipation	+700mW
Rate of Rise of V_{FD}	1.6V/msec.

Electrical Characteristics — Specifications noted only for parameters which change from the S2200/2400 to the S2200A/2400A ($V_{SS} = 0V$, $V_{GG} = 7.5 + 10.0V$, $V_{FD} = V_{GG} + 22V$, $T_A = 0^\circ C$ to $+70^\circ C$. $f_{SYNC} = 125kHz$ to $225kHz$)

	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7 , A_0 thru A_4 High Level Low Level	-3.5		0.6	mA V	$V_{OUT} = V_{FD} - 6V^{**}$ $I = 250\mu A^{**}$
OUTPUTS	A_5 thru A_{12} , EXT, SYNC, & STATUS High Level Low Level	3.5		0.6	V V	$I = -5mA^{**}$ $I = +5mA^{**}$
I_{GG}	Supply Current		28	50	mA	No Loads

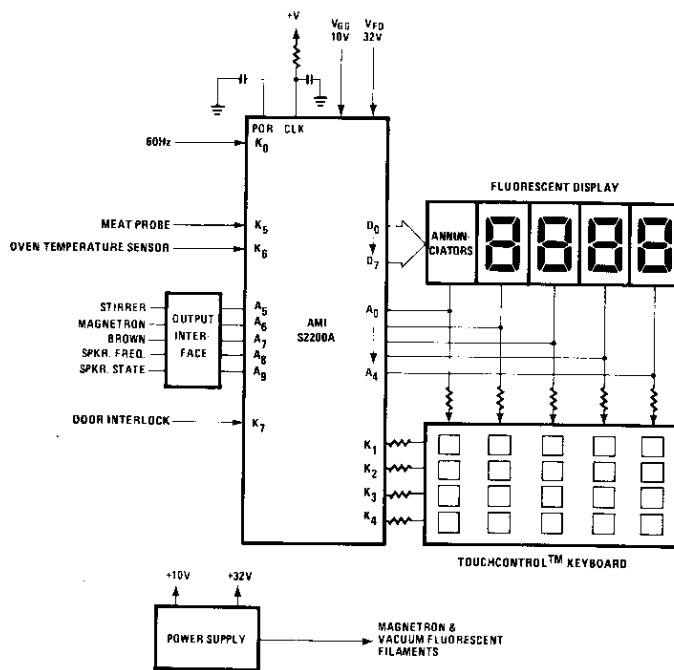
NOTE 1: The output buffers for lines A_5 - A_{12} are supplied from V_{GG} .

**At $V_{GG} \geq 8.5VDC$

NOTE 2: The high voltage parts, when biased with normal V_{FD} , are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

S2000A Typical Microwave Standard Oven Application



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