

Contents

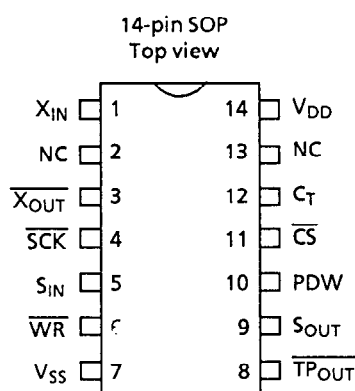
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The S-3520CF is a real time clock that inputs/outputs serial clock or calendar data into/from the CPU. A built-in voltage regulator provides good frequency stability and low power consumption. Even during backup operation, the S-3520CF is effective for saving battery life. It has a built-in 120-bit SRAM, it is also useful for CPU data backup.

■ Features

- Easy serial interface to CPU with 5 lines ($\overline{\text{SCK}}$, S_{IN} , S_{OUT} , $\overline{\text{CS}}$, and $\overline{\text{WR}}$)
- Low current consumption:
3.0 μA max. at $V_{\text{DD}} = 5.0 \text{ V}$ during backup
- Wide data retention voltage range : 2.0 to 6.0 V
- Good frequency stability against fluctuating power supply voltage : $\pm 5 \text{ ppm}$ at $V_{\text{DD}} = 2.0$ to 6.0 V
- Reference signal output can be selected from 1 Hz and 1024 Hz
- Data is serially output in BCD
- Clock and calendar data is modified by increment method
- Built-in auto-calendar until the year 2099
- Built-in counters for clock and calendar
- 30-s adjust function by software
- Built-in 30×4 -bit SRAM
- 14-pin SOP package

■ Pin Assignment



Pin No.	Name	Functions
1	X_{IN}	Input terminal of oscillation circuit
3	X_{OUT}	Output terminal of oscillation circuit
4	$\overline{\text{SCK}}$	Synchronous signal input terminal of serial I/O, 8 clocks/cycle
5	S_{IN}	Serial address/data input terminal Counter address or address/data of register/RAM is input
9	S_{OUT}	Serial address/data output terminal Counter address or address/data of register/RAM is output
6	$\overline{\text{WR}}$	Read/write selection terminal $\overline{\text{WR}} = \text{"L"} : \text{Write}$ $\overline{\text{WR}} = \text{"H"} : \text{Read}$
11	$\overline{\text{CS}}$	Chip select terminal $\overline{\text{CS}} = \text{"L"} : \text{The S-3520CF is selected}$ $\overline{\text{CS}} = \text{"H"} : \text{S}_{\text{OUT}} \text{ becomes high impedance}$
10	PDW	Acknowledge signal input terminal of system power on. Connected to power-down detection circuit. Unless PDW is used, it is fixed to high level. When PDW is low, it cannot be accessed regardless of $\overline{\text{CS}}$, and S_{OUT} and TP_{OUT} become high impedance.
8	TP_{OUT}	Reference signal output terminal, selected from 1Hz/1024Hz
14	V_{DD}	Positive power supply (+5 V, +3 V during backup)
7	V_{SS}	Negative power supply, connected to ground
12	C_{T}	Connects a capacitor of 0.0047 μF between V_{DD} pin and C_{T} pin
2, 13	NC	Not used (set to open)

■ **Block Diagram**

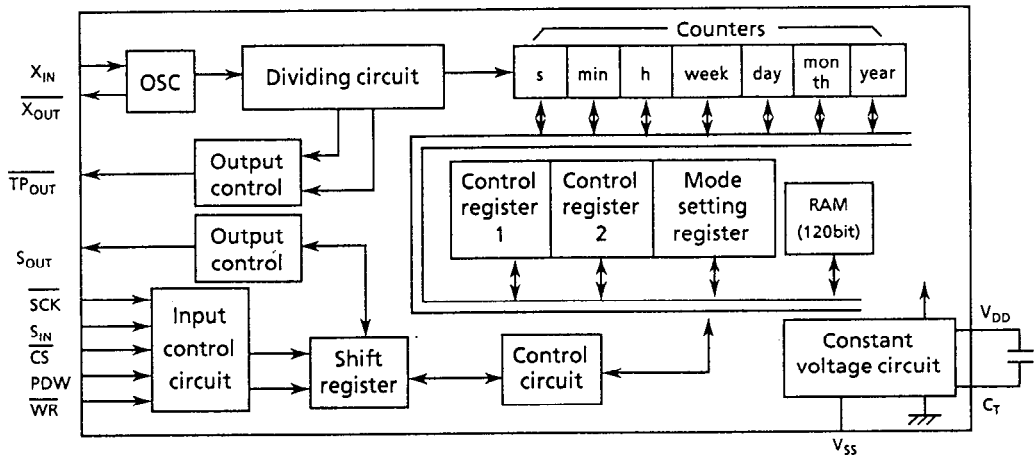


Figure 1

■ **Functions**

1. Address allocation

The S-3520CF reads and modifies the contents of counters, registers, and RAMs, with 4-bit address and data in a set. Their addresses are allocated as in Table 1.

Table 1

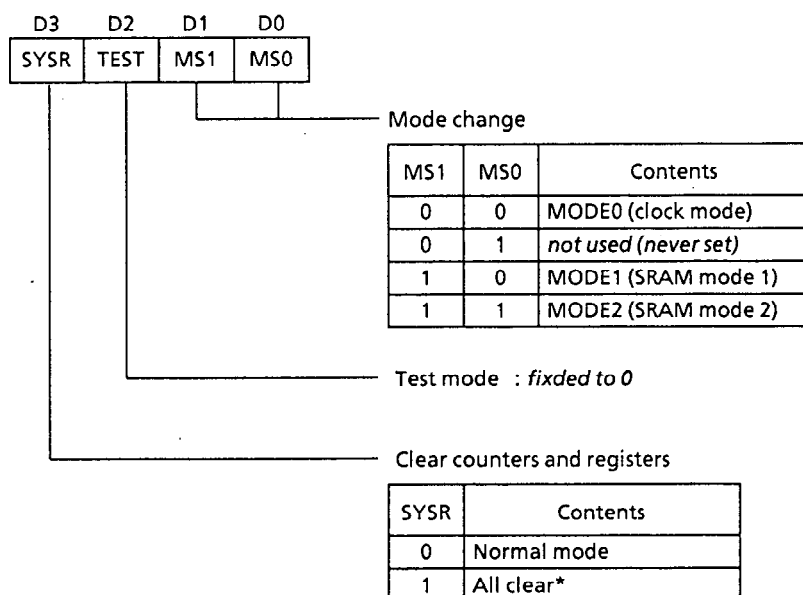
Address (A3 to A0)	Contents		
	MODE0	MODE1	MODE2
0000	1-second digit counter	SRAM RA ₀ to RA ₅₉	SRAM RA ₆₀ to RA ₁₁₉
0001	10-second digit counter		
0010	1-minute digit counter		
0011	10-minute digit counter		
0100	1-hour digit counter		
0101	10-hour digit counter		
0110	Week counter		
0111	1-day digit counter		
1000	10-day digit counter		
1001	1-month digit counter		
1010	10-month digit counter		
1011	1-year digit counter		
1100	10-year digit counter		
1101	Control register 1		
1110	Control register 2		
1111	Mode setting register		

2. Registers

2.1 Mode setting register

The mode setting register changes the mode of the S-3520CF between clock mode (MODE0) and SRAM mode (MODE1 and MODE2), and resets all systems. The register data can be written and read.

Mode setting register (MODE, 1111)



* Cleared contents

Counters	Year:00, month:01, day:01, hour:00**, minute:00, second:00, day of week:00
RAMs	Data remains
Registers	Control registers 1 and 2 : 0 for all bits Mode setting register : 1 for SYSR, 0 for others

** 12 is displayed.

2.2 Control register 1

The control register 1 controls the basic function of the clock mode. Register data can be written and read.

Control register 1 (CNT1, 1101)

D3	D2	D1	D0
TPS	30ADJ	CNTR	24/12

Display mode change

24/12	Contents
0	12-hour system
1	24-hour system

Note: After the display mode is set to the 24-hour system, perform reset.

Reset counter

CNTR	Contents
0	Normal mode
1	Reset setting

The CNTR bit is not a execution bit. The contents of the counter, followed by setting this bit, are reset as follows (see ■ Operation 4.2. (2)):

1-day or 1-month digit counters : 0001

Other counters : 0000

± 30-s adjust bit (one shot, returned within 220 μ s)

30ADJ	Contents
0	Normal mode
1	± 30-s adjust <ul style="list-style-type: none"> When a current time is between 0 to 29 s, digits are reset without carry to min digits When a current time is between 30 to 59 s, digits are reset with carry to min digits

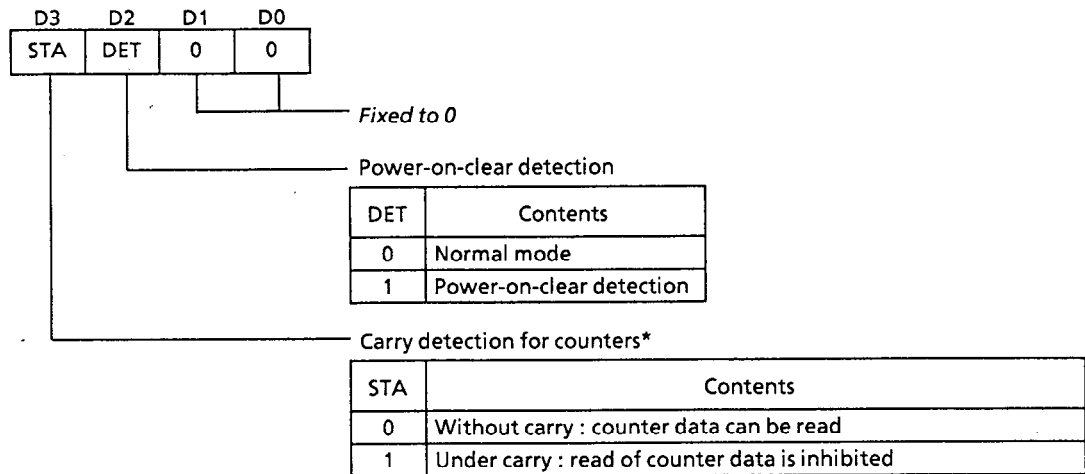
Output waveform selection of reference signal

TPS	Contents
0	1024 Hz
1	1 Hz

2.3 Control register 2

The control register 2 is a flag to detect the status in the clock mode. The register data can be only read.

Control register 2 (CNT2, 1110)



- * When STA is 0, no carry is executed in 3.9 ms after STA was read. If STA becomes 1 while the clock data is being read, erroneous data may be read.

3. Counters

This section describes counters for the clock and calendar, whose data can be read and incremented for modification.

3.1 Second counters

1-second digit counter (sec1, 0000)

D3	D2	D1	D0
S ₈	S ₄	S ₂	S ₁

Counts 0 to 9
Data is carried to the 10-second digit counter

10-second digit counter (sec10, 0001)

D3	D2	D1	D0
0	S ₄₀	S ₂₀	S ₁₀

Counts 0 to 5
Data is carried to the 1-minute digit counter

3.2 Minute counters

1-minute digit counter (min1, 0010)

D3	D2	D1	D0
M ₈	M ₄	M ₂	M ₁

Counts 0 to 9
Data is carried to the 10-minute digit counter

10-minute digit counter (min10, 0011)

D3	D2	D1	D0
0	M ₄₀	M ₂₀	M ₁₀

Counts 0 to 5
Data is carried to the 1-hour digit counter

3.3 Hour counters

1-hour digit counter (hou1, 0100)

D3	D2	D1	D0
H ₈	H ₄	H ₂	H ₁

Counts 0 to 9

Data is carried to the 10-hour digit counter

10-hour digit counter (hou10, 0101)

D3	D2	D1	D0
PM/AM*	0	H ₂₀	H ₁₀

Counts 0 to 2

Data is carried to the 1-day digit and week counters

* PM/AM is output even if time is displayed in the 24-hour system.

3.4 Week counter

Week counter (wee, 0110)

D3	D2	D1	D0
0	W ₄	W ₂	W ₁

Counts 0 to 6

* Decide the correspondance of day of the week and counter value.

3.5 Day counters

1-day digit counter (day1, 0111)

D3	D2	D1	D0
D ₈	D ₄	D ₂	D ₁

Counts 0 to 9

Data is carried to the 10-day digit counter

10-day digit counter (day10, 1000)

D3	D2	D1	D0
0	0	D ₂₀	D ₁₀

Counts 0 to 3

Data is carried to the 1-month digit counter

The auto-calendar function automatically changes the maximum counter value according to the month as follows:

January, March, May, July, August, October, and December ; 31 days

April, June, September, and November ; 30 days

February ; 28 days, but 29 days in leap year

3.6 Month counters

1-month digit counter (mon1, 1001)

D3	D2	D1	D0
MO ₈	MO ₄	MO ₂	MO ₁

Counts 0 to 9

Data is carried to the 10-month digit counter

10-month digit counter (mon10, 1010)

D3	D2	D1	D0
0	0	0	MO ₁₀

Counts 0 to 1

Data is carried to the 1-year digit counter

3.7 Year counters

The year counters set the last 2 digits (00 to 99) of the year. They counts in liaison with the auto-calendar function until the year 2099.

1-year digit counter (yea1, 1011)

D3	D2	D1	D0
Y ₈	Y ₄	Y ₂	Y ₁

Counts 0 to 9

Data is carried to the 10-year digit counter

10-year digit counter (yea10, 1100)

D3	D2	D1	D0
Y ₈₀	Y ₄₀	Y ₂₀	Y ₁₀

Counts 0 to 9

4. SRAM

In MODE1 and MODE2, each of which is selected by the mode setting register, 30×4-bit SRAM data can be written or read. The address and data corresponds as follows.

4.1 MODE1

Address	D3	D2	D1	D0
0000	RA ₃	RA ₂	RA ₁	RA ₀
0001	RA ₇	RA ₆	RA ₅	RA ₄
⋮	⋮	⋮	⋮	⋮
1101	RA ₅₅	RA ₅₄	RA ₅₃	RA ₅₂
1110	RA ₅₉	RA ₅₈	RA ₅₇	RA ₅₆

4.2 MODE2

Address	D3	D2	D1	D0
0000	RA ₆₃	RA ₆₂	RA ₆₁	RA ₆₀
0001	RA ₆₇	RA ₆₆	RA ₆₅	RA ₆₄
⋮	⋮	⋮	⋮	⋮
1101	RA ₁₁₅	RA ₁₁₄	RA ₁₁₃	RA ₁₁₂
1110	RA ₁₁₉	RA ₁₁₈	RA ₁₁₇	RA ₁₁₆

■ Operation

1. Read data

When \overline{CS} goes low, and a serial address is input from S_{IN}, the address is fetched at the rise of the \overline{SCK} clock. Set high for \overline{WR} to select the read mode. When \overline{WR} is fetched at the rise of the 8th \overline{SCK} clock, input address and data is output in the following cycle from S_{OUT}, synchronized with the fall of the \overline{SCK} clock. Figure 3 shows the read timing.

Note When the \overline{SCK} clock is less than 8, the S-3520CF waits for command.

When the \overline{SCK} clock is 9 or more, it executes the command for the first 8 clocks, then waits until 8 more clocks are completed.

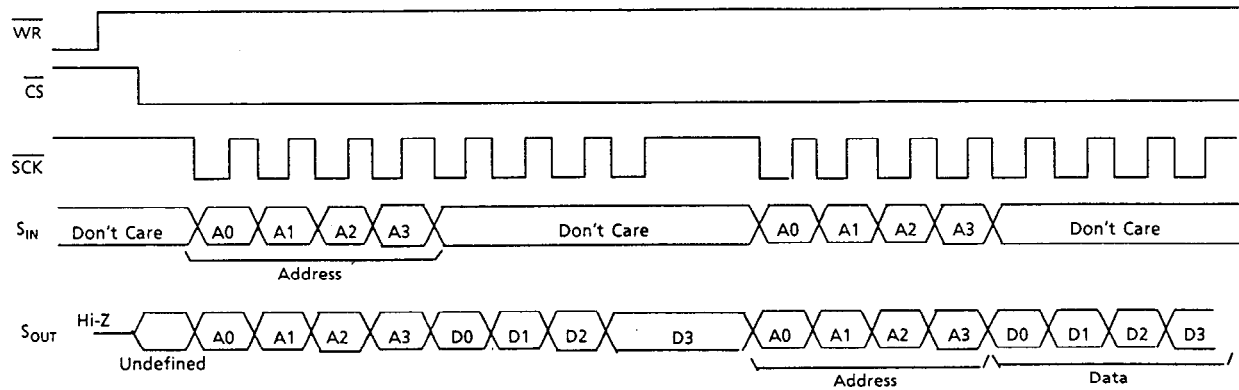


Figure 3 Read timing

2. Write data

When \overline{CS} goes low, and serial address and data (only when written into registers and SRAMs) are input from S_{IN} ; they are fetched at the rise of the \overline{SCK} clock. Set low for \overline{WR} to select the write mode. When \overline{WR} is fetched at the rise of the 8th \overline{SCK} clock, the following data is written in the input address.

- Counters : data incremented by 1
- Registers and SRAMs : 4-bit data input from S_{IN}

This data is output from S_{OUT} in the following cycle, synchronized with the fall of the \overline{SCK} cycle. Figures 4 and 5 show the write timing.

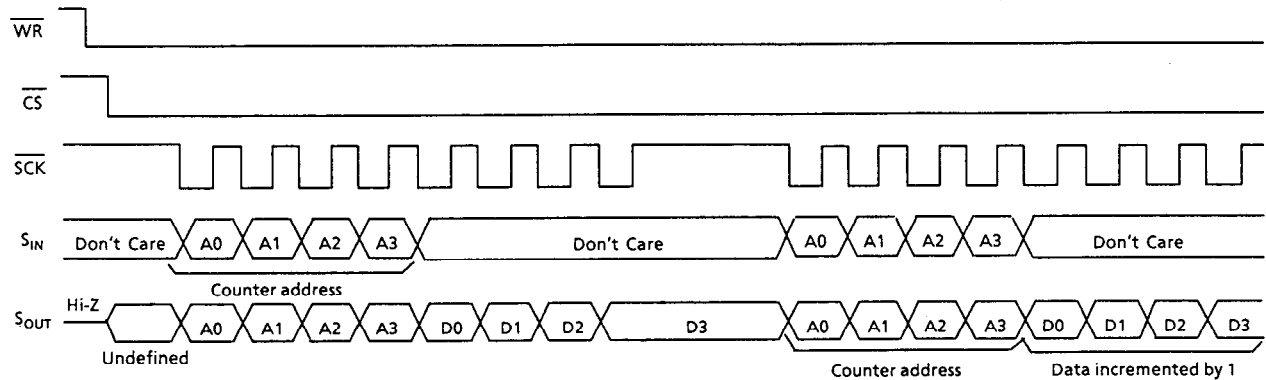


Figure 4 Write timing in clock mode

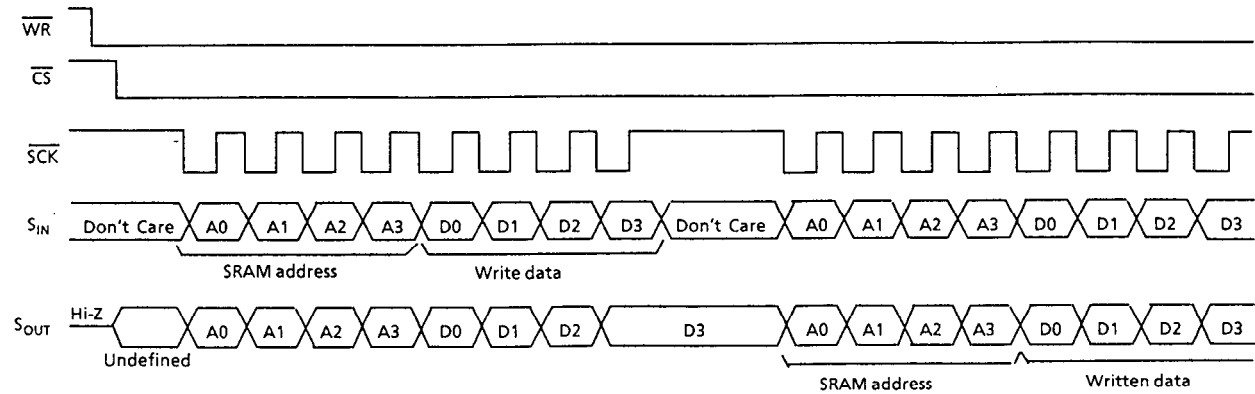


Figure 5 Write timing in SRAM mode

3. Initializing

3.1 Power-on-clear

When power is applied ON, the power-on-clear function is automatically executed to initialize all the logic of the S-3520CF. When power-on-clear is valid, the DET bit (D2 of the control register 2) goes to 1. Return it to 0 by system reset and set each clock and calendar data. Figure 6 shows the conditions where power-on-clear is valid at power on, and where data remains and IC operates normally at power fluctuation.

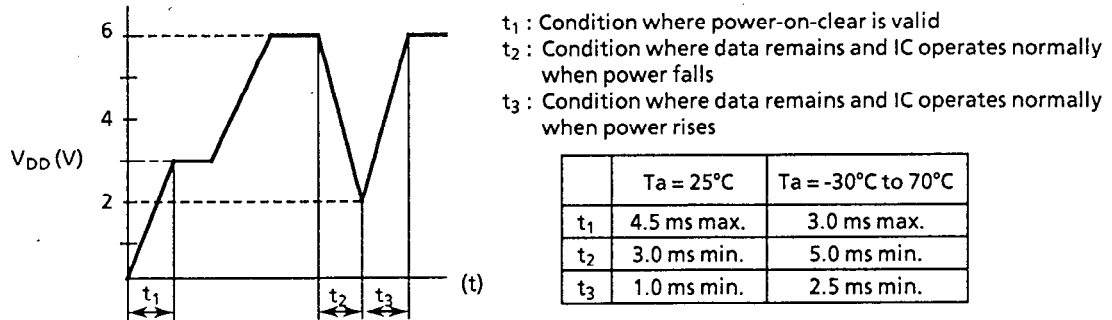


Figure 6 Power-on-clear timing

3.2 System reset

Set 1 for the SYSR bit (D3 of the mode setting register) to initialize all the logic of the S-3520CF. When releasing system reset, input $\overline{\text{SCK}}$ after rise and fall of $\overline{\text{CS}}$ as in Figure 7.

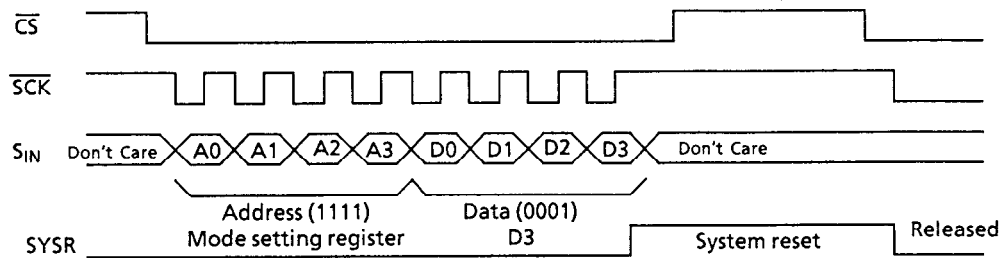


Figure 7 Reset release timing

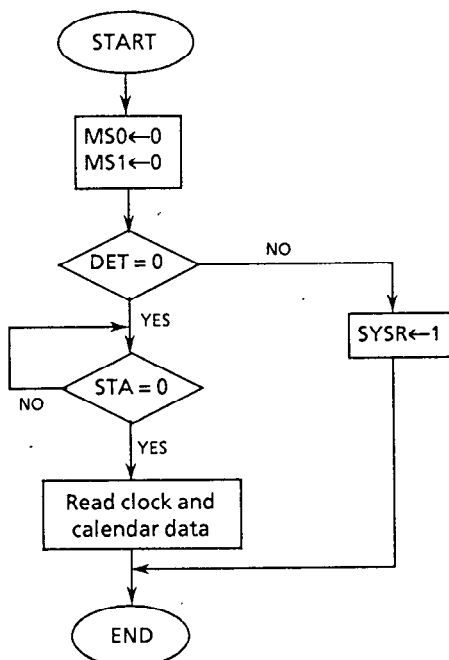
Table 1 Status under initialization

Item	Power-on-clear	System reset
Counters	Year:00, month:01, day:01, hour:00 (12 on display), minute:00, second:00, day of week:00	
SRAMs	Data undefined	Data remained
Registers	1 only for DET	1 only for SYSR

After initialization, when in clock mode, set the initial data (see the next page 4.2) and start to count.

4. Clock mode

4.1 Data read flowchart



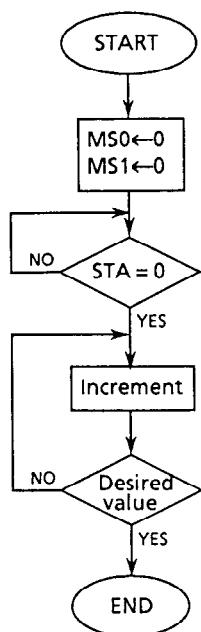
1. Set the S-3520CF in clock mode (MODE0) with the lower 2 bits of the mode setting register
2. When DET is 1, reading is inhibited. Perform system reset to set 0 for DET.
3. Data cannot be read when being carried. So, check that STA is 0, which indicates that carry is not being performed.
4. Read operation starts (see "1. Read Data").

Note When STA is 0, no carry is executed 3.9 ms after STA was read. If STA becomes 0 while the clock data is being read, erroneous data may be read.

4.2 Modification flowchart

There are two methods: one is increment from the current time, and another is the reset and increment from 0. After initialization, set the desired time with the latter method and start to count.

(1) When modifying from current time

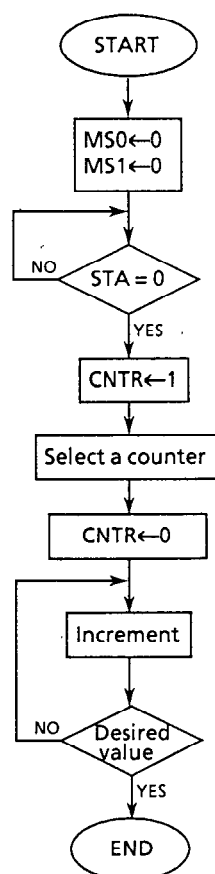


1. Set the S-3520CF in clock mode (MODE0) with the lower 2 bits of the mode setting register.
2. Check that STA is 0, which indicates that carry is not being performed.
Reason: During modification, usual carry from the lower digit counter is accepted. If carry is generated in a 1-digit counter while a 10-digit counter is being carried, the 10-digit counter may accept both carries.
3. Increase one by one until the desired value is obtained.

Note

- In month and year counters, modification may have nonexistent data generated, for which the lower digits are not adjusted. In February, check whether it is in a leap year.
Example: Increment of month counters in "January (01), 31" results in "February (02), 31".
- If minute counters are modified, recommend to set 1 for 30ADJ (D2 of the control register 1) for 30-s adjust, because the second counters have great influence.

(2) When resetting and modifying from 0



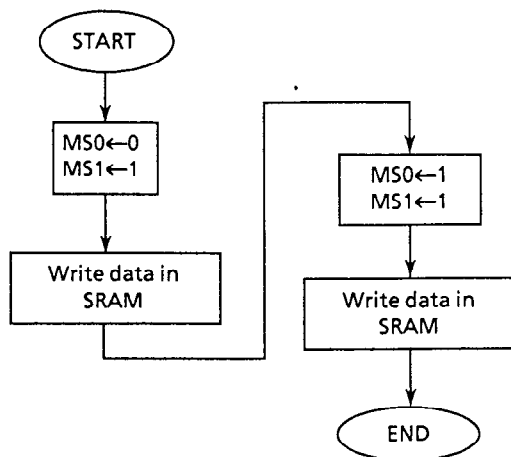
1. Set the S-3520CF in clock mode (MODE0), with lower 2 bits of the mode setting register.
2. Check that STA is 0, which indicates that carry is not being performed.
Reason: During modification, usual carry from the lower digit counter is accepted. If carry is generated in a 1-digit counter while a 10-digit counter is being carried, the 10-digit counter may accept both carries.
3. Set 1 for CNTR to instruct reset of the counter value selected successively.
4. Input the address of the counter you reset.
5. Set 0 for CNTR to return into normal mode.
6. Increase one by one until the desired value is obtained.

Note

- 1-digit and 10-digit counters cannot be reset simultaneously. If both counters must reset, reset one after another.
- In case of 10 of month or 10 of day, if the 10-digit counter is reset, non-existent data such as 0 of month or 0 of day is generated. Do not fail to set data for the 1-digit counter.
- If the minute counters are modified, recommend setting 1 for 30ADJ (D2 of the control register 1) for 30-s adjust, because the second counters have great influence.

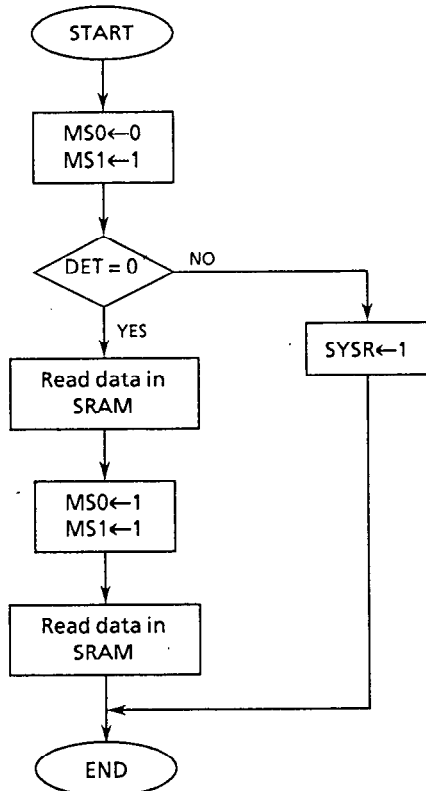
5. SRAM mode

5.1 Write operation flowchart



1. Set the S-3520CF in SRAM mode 1 (MODE1, RA0 to RA59) with the lower 2 bits of the mode setting register.
2. Write data in 4-bit units (see "2. Write Data").
3. Operate in MODE2 (RA60 to RA119), exactly as in MODE1.

5.2 Read operation flowchart



1. Set the S-3520CF in SRAM mode 1 (MODE1, RA₀ to RA₅₉) with the lower 2 bits of the mode setting register.
2. When DET is 1, reading is inhibited. Perform system reset to set 0 for DET.
3. Read data in 4-bit units (see "1. Read Data").
4. Operate in MODE2 (RA₆₀ to RA₁₁₉), exactly as in MODE1.

■ Absolute Maximum Ratings

Table 2

Unless otherwise specified: Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{DD} -V _{SS}		-0.3 to +6.5	V
Input voltage	V _{IN}	SCK, WR, CS, PDW, C _T	-0.3 to V _{DD} + 0.3	V
Output voltage	V _{OUT}	S _{OUT}	-0.3 to +6.5	V
Power dissipation	P _d		200	mW
Storage temperature	T _{stg}		-55 to +125	°C
Operating temperature	T _{opr}		-30 to +75	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V _{DD}		4.0	5.0	6.0	V
Operating temperature	T _{opr}		-30	—	75	°C

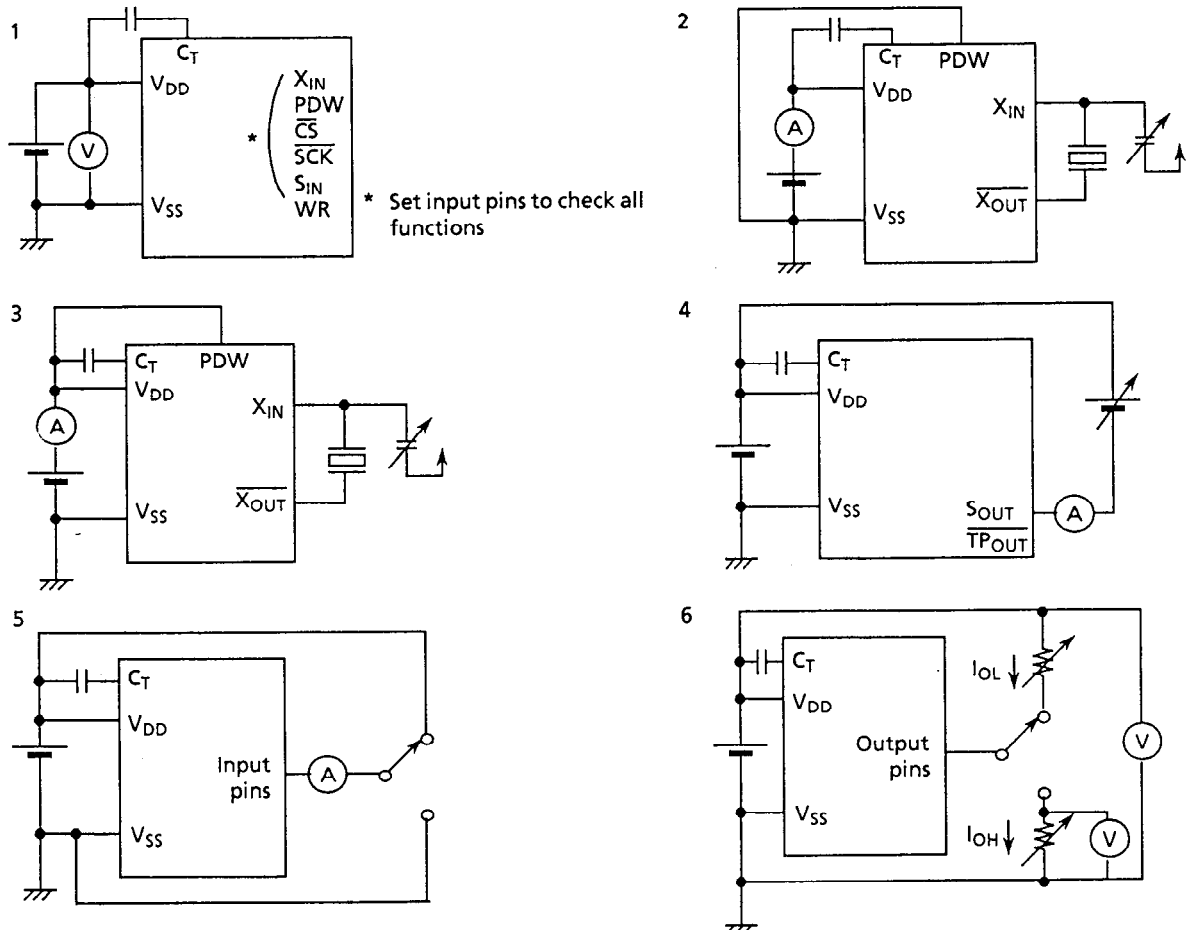
DC Electrical Characteristics

Table 4

Unless otherwise specified : Ta = -30°C to +75°C,
V_{DD} = 5 V ± 10%, V_{SS} = 0 V, C_G = 12 pF
Crystal : DS-VT-200 (32.768 kHz, CL = 6 pF, ± 20 ppm) of
Seiko Instruments Inc,

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Circuit
Power supply voltage	V _{DD}		3.0	5.0	6.0	V	1
Data retention voltage	V _{DH}		2.0	—	6.0	V	1
Current consumption	I _{DD1}	SCK = 500 kHz	—	30	100	μA	3
	I _{DD2}	SCK = V _{DD}	—	2.0	3.0	μA	2
High level output voltage	V _{OH1}	CMOS: I _{OH} = -100 μA	V _{DD} -0.3	—	—	V	6
	V _{OH2}	TTL: I _{OH} = -400 μA	2.4	—	—	V	6
Low level output voltage	V _{OL1}	CMOS: I _{OL} = 100 μA	—	—	0.1	V	6
	V _{OL2}	TTL: I _{OL} = 1.6 mA	—	—	0.4	V	6
Output leakage current	I _{OZH}	V _{OUT} = 5.5 V	-2.0	—	2.0	μA	4
	I _{OZL}	V _{OUT} = 0 V	-2.0	—	2.0	μA	4
Input voltage	V _{IH}		0.8 × V _{DD}	—	—	V	1
	V _{IL}		—	—	0.2 × V _{DD}	V	1
Input leakage current	I _{IZH}	V _{IN} = 5.5 V	-2.0	—	2.0	μA	5
	I _{IZL}	V _{IN} = 0 V	-2.0	—	2.0	μA	5
Oscillation start time	t _S	Ta = 25°C	—	—	3	s	3
Oscillation start voltage	V _{STR}	t _S = 10 s, Ta = 25°C	2.0	—	—	V	3
Oscillation frequency deviation	Δf _{ic}	Deviation between ICs, Ta = 25°C	-15	—	15	ppm	3
Oscillation frequency-voltage deviation	Δf _v	V _{DD} = 2 to 6 V, Ta = 25°C	-5	—	5	ppm	3
High/low range	—	C _G = 5 to 30 pF	30	—	—	ppm	3
External capacity of oscillator	C _G		3	11	35	pF	—
Built-in capacity of oscillator	C _D		—	13.4	—	pF	—

Measuring Circuits



■ AC Electrical Characteristics

Table 5

Unless otherwise specified :

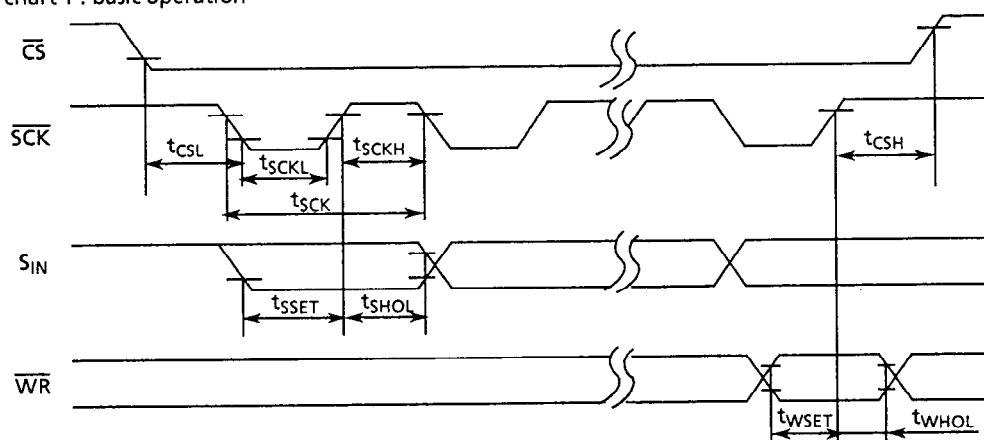
$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -30^\circ C$ to $+75^\circ C$, $C_G = 12\text{ pF}$

Input pins : $V_{IH} = 0.8 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$

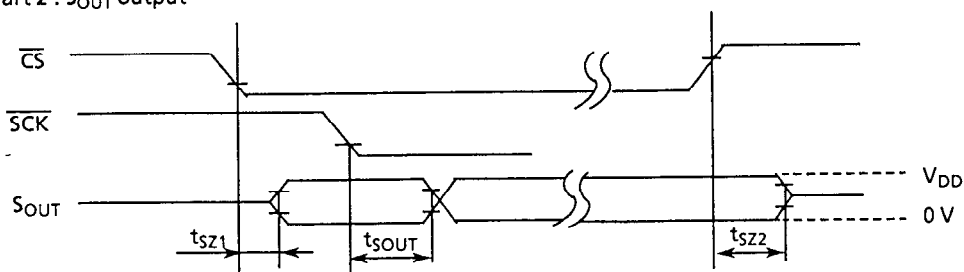
Output pins : $V_{OH} = 0.8 \times V_{DD}$, $V_{OL} = 0.2 \times V_{DD}$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Chart
SCK period	t_{SCK}		2.0	—	—	μs	1
Low period of \overline{SCK}	t_{SCKL}		1.0	—	—	μs	1
High period of \overline{SCK}	t_{SCKH}		1.0	—	—	μs	1
Time from fall of \overline{CS} to fall of \overline{SCK}	t_{CSL}		5.0	—	—	μs	1
Time from rise of \overline{SCK} to rise of \overline{CS}	t_{CSH}		220	—	—	μs	1
S_{IN} setup time	t_{SSET}		1.0	—	—	μs	1
S_{IN} hold time	t_{SHOL}		1.0	—	—	μs	1
\overline{WR} setup time	t_{WSET}		5.0	—	—	μs	1
\overline{WR} hold time	t_{WHOL}		5.0	—	—	μs	1
Time from fall of \overline{SCK} to S_{OUT} output	t_{SOUT}	$CL = 100\text{ pF}$	—	300	500	ns	2
Time from fall of \overline{CS} to S_{OUT} output	t_{SZ1}	$CL = 100\text{ pF}$	—	—	100	ns	2
Time from rise of \overline{CS} to S_{OUT} output	t_{SZ2}	$CL = 100\text{ pF}$	—	—	100	ns	2
Time from rise of \overline{PDW} to S_{OUT} output	t_{SZ3}	$CL = 100\text{ pF}$	—	—	100	ns	3
Time from fall of \overline{PDW} to High-Z of S_{OUT}	t_{SZ4}	$CL = 100\text{ pF}$	—	—	100	ns	3
Time from rise of \overline{PDW} to \overline{TP}_{OUT} output	t_{TZ1}	$CL = 100\text{ pF}$	—	—	100	ns	3
Time from fall of \overline{PDW} to High-Z of \overline{TP}_{OUT}	t_{TZ2}	$CL = 100\text{ pF}$	—	—	100	ns	3
SCK pause time	t_{SPS}		220	—	—	μs	4
\overline{CS} pause time (at system reset release)	t_{CPC}		2.0	—	—	μs	5

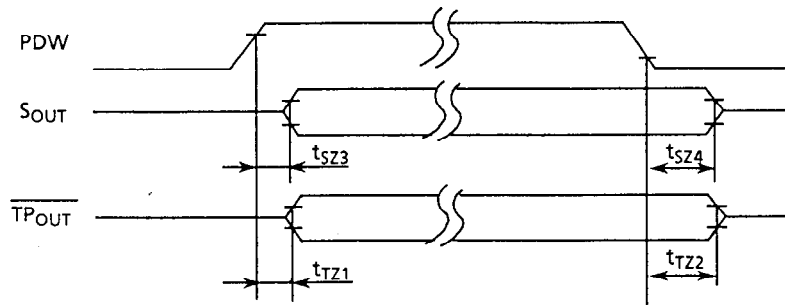
• Timing chart 1 : basic operation



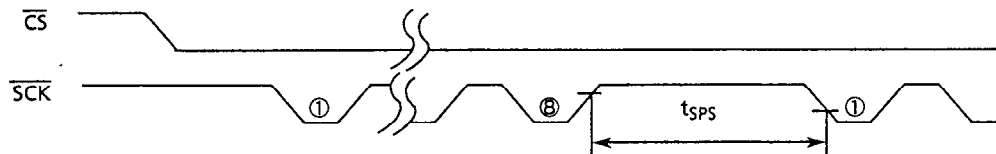
• Timing chart 2 : S_{OUT} output



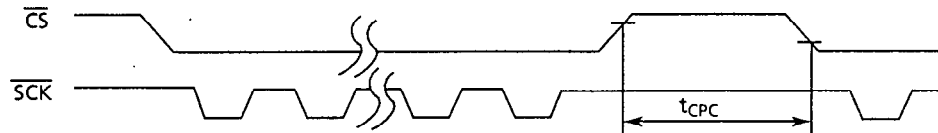
- Timing chart 3 : power down



- Timing chart 4 : pause time



- Timing chart 5 : system reset release



■ Application Circuit Design

1. Peripheral circuit of PDW and \overline{CS}

When PDW is low, any input cannot be accepted, and S_{OUT} and $\overline{TP_{OUT}}$ become high impedance. When PDW and \overline{CS} are high, any input cannot be accepted, and S_{OUT} becomes high impedance. Figure 8 shows the internal circuits of the input block of PDW and \overline{CS} .

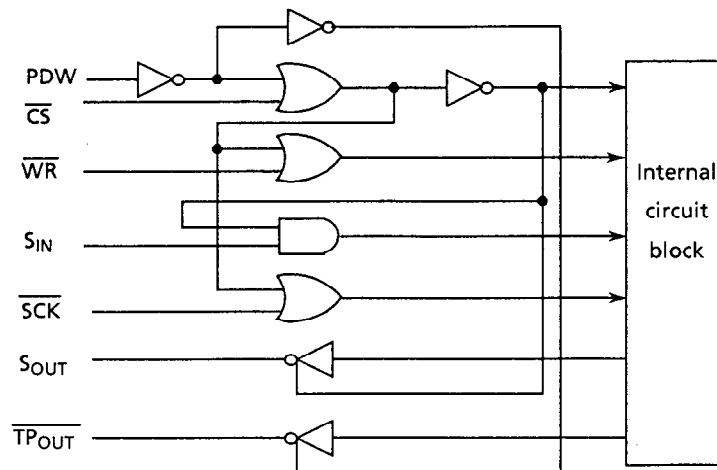


Figure 8

2. When using a single power source

After power turns on, the S-3520CF can interface with CPU according to the timing of Figure 9. That is, after PDW goes high, \overline{CS} stays high for 3 s min. until the oscillation circuit rises. Then, \overline{CS} goes low to start interfacing.

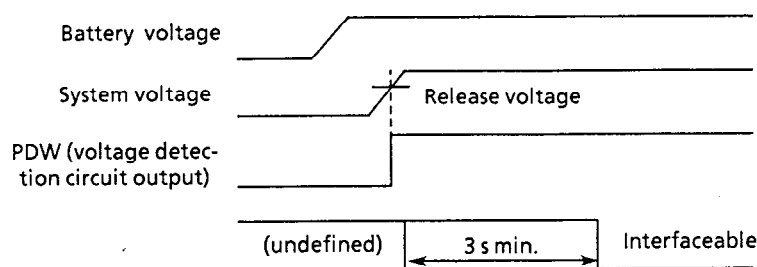


Figure 9

Note When PDW is low, keep PDW in a high or low status, never in a floating status. If PDW is in a floating status, a through-type current may flow to hasten current deterioration.

3. When using two power sources

Figure 10 shows an example circuit using two power sources.

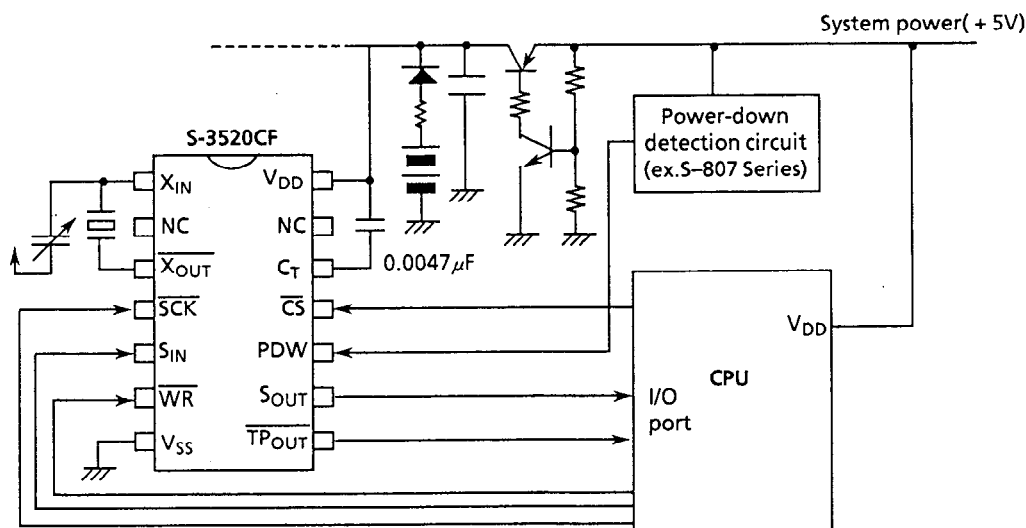
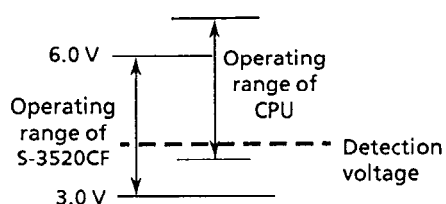


Figure 10

When using the S-3520CF with system power and backup battery power, power-down detection and power change circuits are needed. If the system power is down, V_{DD} falls to the battery voltage level. The power supply voltage range where the S-3520CF can interface with a CPU is 3.0 to 6.0 V. To prevent a malfunction, design a circuit so that the S-3520CF cannot be accessed when V_{DD} is higher than 3.0 V and higher than the minimum operating voltage of the CPU (see Figure 11). As in Figure 12 on the next page, moreover, design so that the PDW goes low before V_{DD} falls to (1) and goes high after system power returns and V_{DD} rises to (1).

(1) Minimum operating voltage of the CPU ≥ 3.0 V



(2) Minimum operating voltage of the CPU < 3.0 V

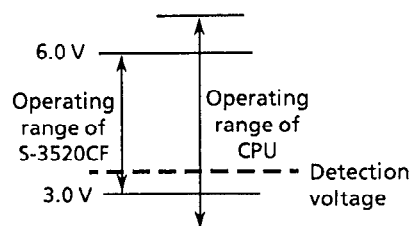


Figure 11 Setting of detection voltage at power down of system power

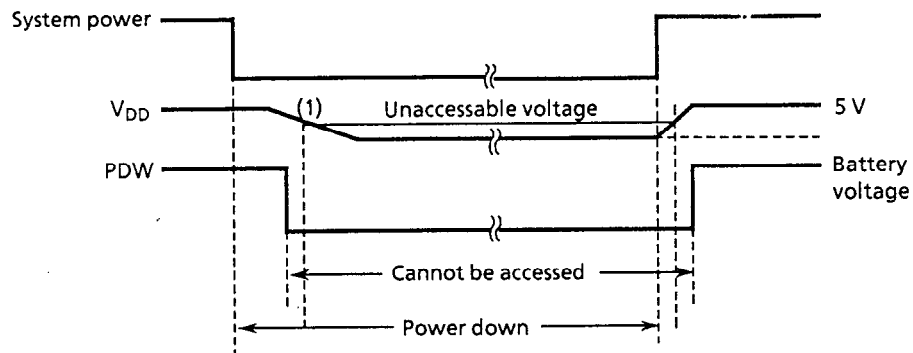
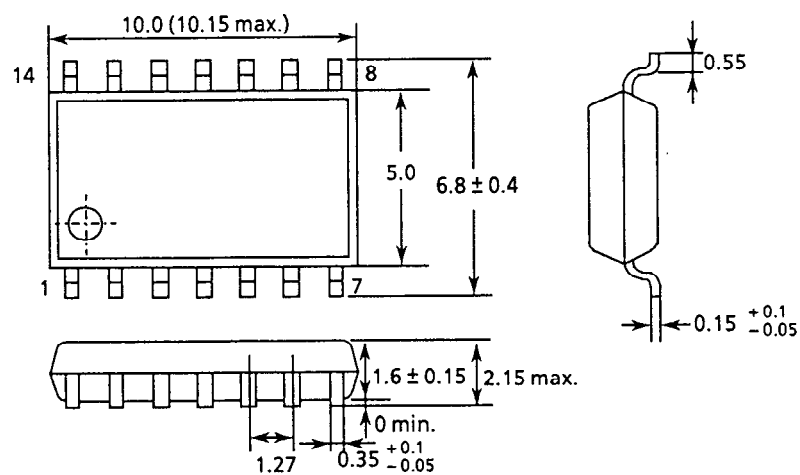


Figure 12

Note When interfacing with the CPU, system power is down (battery power is on) to send the PDW low, data under accessing is invalid. When the system power is restored, a data output from S_{OUT} in a cycle just after PDW goes high is undefined.

■ Dimensions

14-pin SOP



Unit : mm

Figure 13