H0488
Parallel Input Dot Matrix LCD Driver

HUGHES AIRCRAFT COMPANY
SEMICONDUCTOR DIVISION
Industrial Electronics Group

DESCRIPTION

Hughes 0488 is a CMOS/LSI circuit that drives a rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns. The 0488 is organized as 16 rows and 16 columns. It will drive an LCD display of up to 16 x 16 directly and can be cascaded for larger displays.

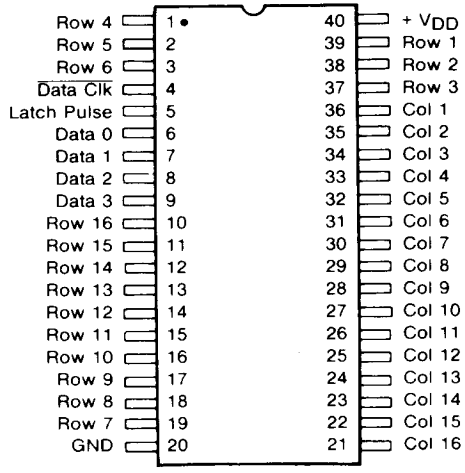
Data is input 4 bit parallel to minimize the time required to load in data. This circuit drives (using a multiplexed scheme) the display with proper voltage level waveforms, but does not handle refresh, character encoding, or AC generation. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0488 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for large displays
- On chip precision voltage divider
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and PMOS compatible inputs
- Architecture allows arbitrary display patterns
- 4 bit parallel input

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

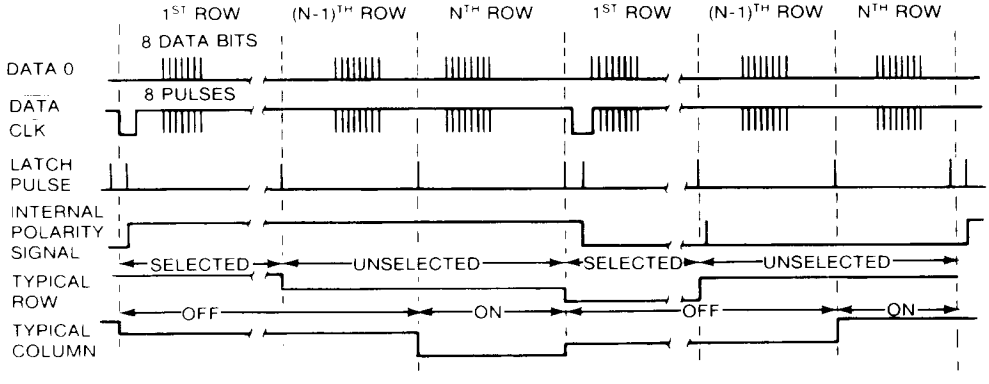
V_{DD} ..... — .3 to + 17 Volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 Volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C
Storage Temperature ..... — 65 to + 125°C

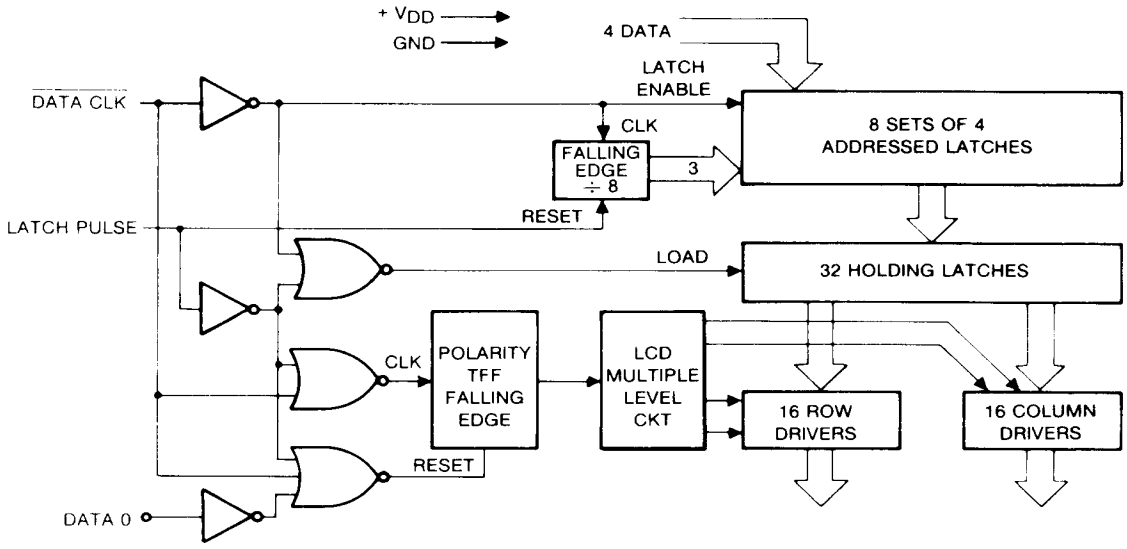
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

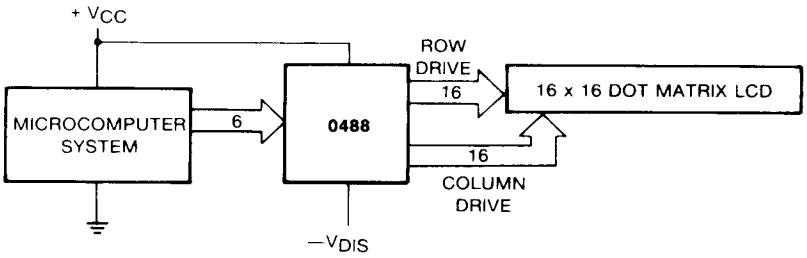
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	8	V
Supply Current	I_{DD}			1.5	mA
Input High Level	V_{IH}		V_{DD}—.5	V_{DD}	V
Input Low Level	V_{IL}		—12	V_{DD}—2	V
Input Leakage	I_L			5	μA
Input Capacitance	C_I			5	pf
Output High Selected	V_{OH}		V_{DD}—.05	V_{DD}	V
Output Low Selected	V_{OL}		0	.05	V
Output High Unselected	$V_{2/3}$		2/3 V_{DD}—.05	2/3 V_{DD} + .05	V
Output Low Unselected	$V_{1/3}$		1/3 V_{DD} —.05	1/3 V_{DD} + .05	V
Row and Column Output Impedence	R_{ON}	I_L = 10μA		15	KΩ
Data in Setup Time	t_{DS}	Data Change to clock fall		500	nsec
Data in Hold Time	t_{DH}	Clock Fall to data change		250	nsec
Latch Pulse Width	t_{PW}			500	nsec

TYPICAL WAVEFORMS





TYPICAL SYSTEM BLOCK DIAGRAM USING 0488



OPERATING NOTES

1. The addressed latches load when $\overline{\text{Data Clk}}$ is low.
2. A logic 1 on Data In selects a row or causes a segment to be visible.
3. A parallel transfer of data from the addressed latches to the holding latches occurs whenever Latch Pulse is high and $\overline{\text{Data Clk}}$ is high.
4. Output drive polarity is inverted upon the falling edge of Latch Pulse if $\overline{\text{Data Clk}}$ is low.
5. Latch Pulse, when high, resets the ÷ 8 latch address counter.
6. When they are selected Row and Column waveforms are full swing and out of phase with each other. Unselected rows swing from 1/3 to 2/3 of supply out of phase with a selected row waveform. Unselected columns operate analogously.
7. The intended mode of operation is as follows: (see timing diagram)
   A. The Polarity signal (internal to circuit) has a frequency slightly above the flicker rate. 30Hz to 50Hz is adequate.
   B. The Polarity signal should be a square wave of precisely 50% duty cycle to keep DC off the display.
   C. The latch pulse is exactly periodic with a frequency of Polarity frequency x 2 x number of backplanes utilized, plus 2 extra pulses per Polarity period. These extra pulses are associated with a change of Polarity. The state of $\overline{\text{Data Clk}}$ must change from high to low between these first and second closely spaced pulses.
   D. Each time increment contains 8 rising edges of $\overline{\text{Data Clk}}$.
8. To synchronize two circuits driving a large display, set Latch Pulse and Data 0 high with $\overline{\text{Data Clk}}$ low, drop Data 0, then begin normal timing. This initializes the Polarity FF.
9. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
10. Input order of 0488:

Clk Pulse	1	2	3	4	5	6	7	8
Data 0	R 1	R 5	R 9	R 13	C 1	C 5	C 9	C 13
Data 1	R 2	R 6	R 10	R 14	C 2	C 6	C 10	C 14
Data 2	R 3	R 7	R 11	R 15	C 3	C 7	C 11	C 15
Data 3	R 4	R 8	R 12	R 16	C 4	C 8	C 12	C 16

11. The RMS drive voltages supplied by this IC to an N backplane LCD are as follows:

$$V_{OFF} = V_{DD}/3 \qquad V_{ON} = \frac{V_{DD}}{3}\sqrt{\frac{N+8}{N}}$$

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