HUGHES
HUGHES AIRCRAFT COMPANY
SOLID STATE PRODUCTS

PARALLEL INPUT DOT MATRIX LCD DRIVER

HLCD 0488

DESCRIPTION

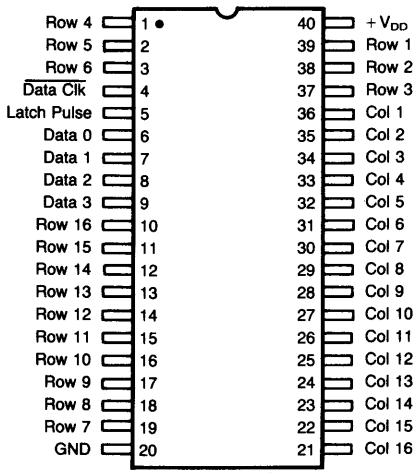
The HLCD 0488 is a CMOS/LSI circuit that drives rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns. The HLCD 0488 is organized as 16 rows and 16 columns. It will drive an LCD display of up to 16 X 16 directly and can be cascaded for larger displays.

Data is input 4 bit parallel to minimize the time required to load in data. This circuit could be referred to as a dumb driver because it drives (using a multiplexed scheme) the display with proper voltage level waveforms, but does not handle refresh, character encoding, or AC generation. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for large displays
- On chip precision voltage divider
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and PMOS compatible inputs
- Architecture allows arbitrary display patterns
- 4 bit parallel input

PIN CONFIGURATION



HLCD 0488

MAXIMUM RATINGS

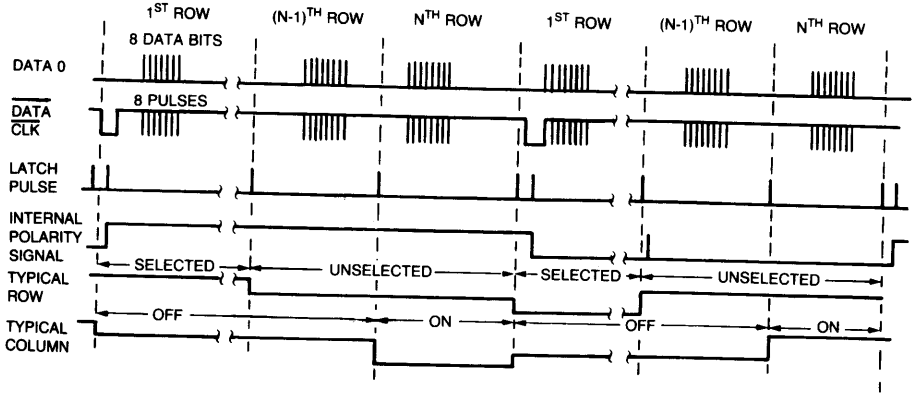
V_{DD} ..... −.3 to 17 volts
Inputs ..... $+V_{DD}$ −17 to $+V_{DD}$ +.3 volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... −55 to +125°C
Plastic Package ..... −40 to +85°C
Storage Temperature ..... −65 to +125°C

ELECTRICAL CHARACTERISTICS

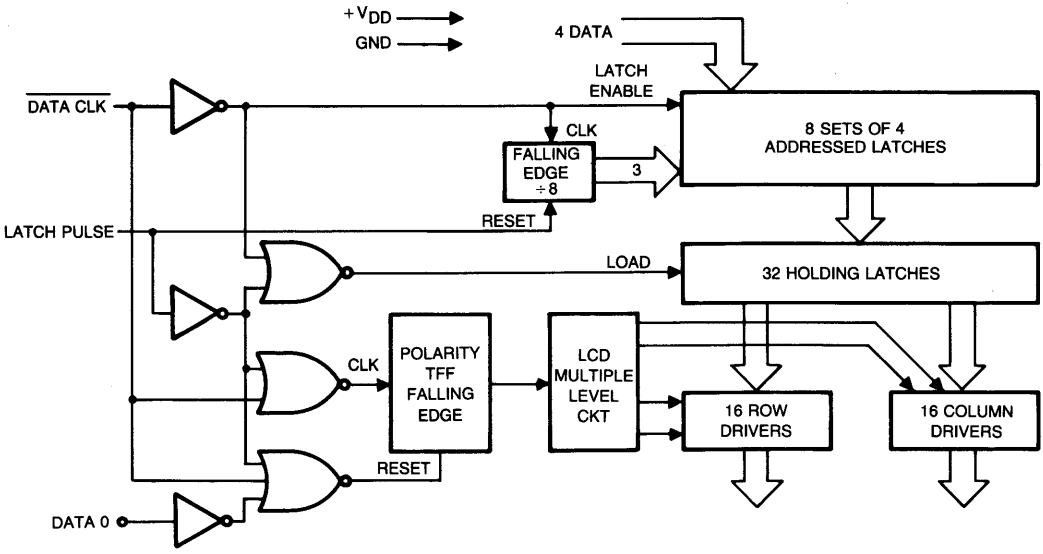
T = 25° and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNITS
Supply Voltage Supply Current	V_{DD} I_{DD}		3	8 1.5	V mA
Input High Level Input Low Level Input Leakage Input Capacitance	V_{IH} V_{IL} I_L C_I		V_{DD}−.5 −12	V_{DD} V_{DD}−2 5 5	V V µA pf
Output High Selected Output Low Selected	V_{OH} V_{OL}		V_{DD}−.05 0	V_{DD} .05	V V
Output High Unselected Output Low Unselected	V_{23} V_{13}		$2/3V_{DD}$−.05 $1/3V_{DD}$−.05	$2/3V_{DD}$+.05 $1/3V_{DD}$+.05	V V
Row and Column Output Impedance	R_{on}	I_L = 10µA		15	KΩ
Data in Setup Time Data in Hold Time Latch Pulse Width	t_{ds} t_{dh} t_{pw}	Data change to clock fall Clock Fall to data change		500 250 500	nsec nsec nsec

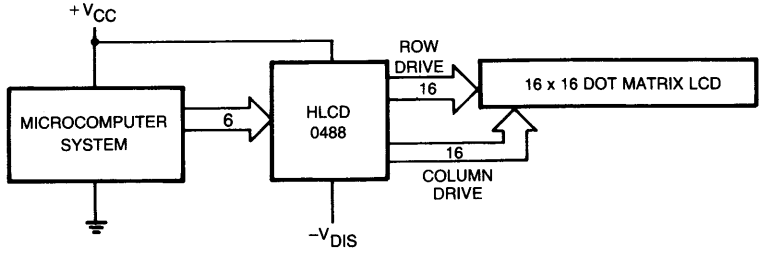
TYPICAL WAVEFORMS



BLOCK DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM USING HLCD 0488



OPERATING NOTES

1. The addressed latches load when $\overline{\text{Data Clk}}$ is low.
2. A logic 1 on Data In selects a row or causes a segment to be visible.
3. A parallel transfer of data from the addressed latches to the holding latches occurs whenever Latch Pulse is high and $\overline{\text{Data Clk}}$ is high.
4. Output drive polarity is inverted upon the falling edge of Latch Pulse if $\overline{\text{Data Clk}}$ is low.
5. Latch Pulse, when high, resets the ÷ 8 latch address counter.
6. When they are selected, Row and Column waveforms are full swing and out of phase with each other. Unselected rows swing from ⅓ to ⅔ of supply out of phase with a selected row waveform. Unselected columns operate analogously.
7. The intended mode of operation is as follows: (see timing diagram)
   A. The Polarity signal (internal to circuit) has a frequency slightly above the flicker rate. 30Hz to 50Hz is adequate.
   B. The Polarity signal should be a square wave of precisely 50% duty cycle to keep DC off the display.
   C. The latch pulse is exactly periodic with a frequency of Polarity frequency x 2 x number of backplanes utilized, plus 2 extra pulses per Polarity period. These extra pulses are associated with a change of Polarity. The state of Data Clk must change from high to low between these first and second closely spaced pulses.
   D. Each time increment contains 8 rising edges of $\overline{\text{Data Clk}}$.
8. To synchronize two circuits driving a large display, set Latch Pulse and Data 0 hi with $\overline{\text{Data Clk}}$ low, then drop Data 0, then begin normal timing. This initializes the Polarity FF.
9. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
10. Input order of HLCD 0488:

Clk Pulse	1	2	3	4	5	6	7	8
Data 0	R1	R5	R9	R13	C1	C5	C9	C13
Data 1	R2	R6	R10	R14	C2	C6	C10	C14
Data 2	R3	R7	R11	R15	C3	C7	C11	C15
Data 3	R4	R8	R12	R16	C4	C8	C12	C16

11. The RMS drive voltages supplied by this IC to an N backplane LCD are as follows:

$$V_{OFF} = V_{DD}/3 \qquad V_{ON} = \frac{V_{DD}}{3}\sqrt{\frac{N+8}{N}}$$

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In Europe: Hughes Solid State Products

Supercedes Previous Data