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Serial Input Dot Matrix LCD Driver

HLCD 0607A

DESCRIPTION

The HLCD 0607A is a CMOS/LSI circuit that drives a matrix LCD display under microcomputer control. The intended display is a 4 × 4 (16 segment) alphanumeric matrix or a 4 × 2 or 3 × 3 numeric matrix, each with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this circuit.

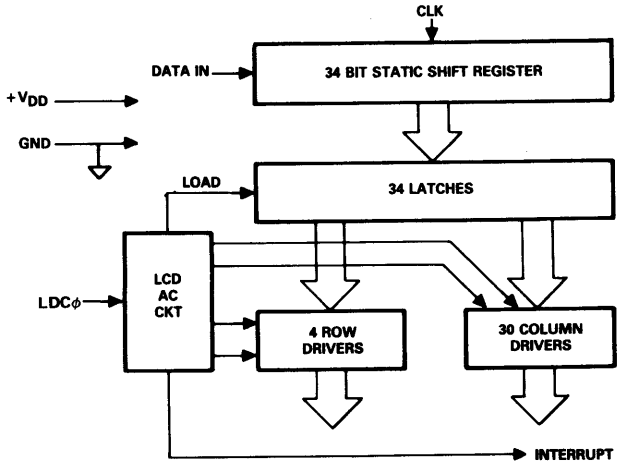
The HLCD 0607A is organized as 4 rows × 30 columns, and thus can handle 7 alphanumeric or 15 numeric characters by itself. The HLCD 0539A, organized as 0 rows × 34 columns may be used in addition to the HLCD 0607A when more than 30 columns are required. Data is serially input to maximize the number of output pins and minimize the number of control pins. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The HLCD 0607A is available in a 40 lead dual-in-line ceramic (D suffix) or plastic (P suffix) package. Unpackaged dice (H suffix) are available upon request.

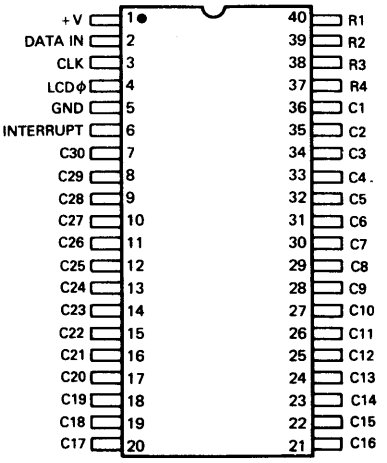
FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt output to request data from microcomputer

BLOCK DIAGRAM



PIN CONFIGURATION



HLCD 0607

MAXIMUM RATINGS

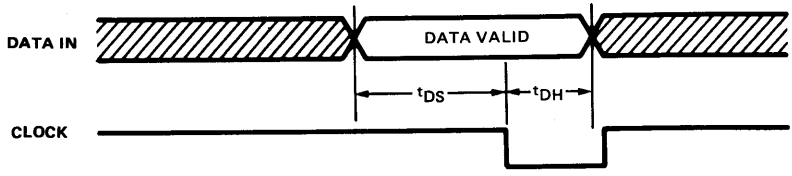
V_{DD} ..... −.3 to 15 volts
Inputs ..... $+V_{DD}-17$ to $+V_{DD}+.3$ volts
Power Dissipation ..... 250 mW
Storage Temperature ..... −65 to +125°C
Operating Temperature
Ceramic Package ..... −55 to +125°C
Plastic Package ..... −40 to +85°C

ELECTRICAL CHARACTERISTICS

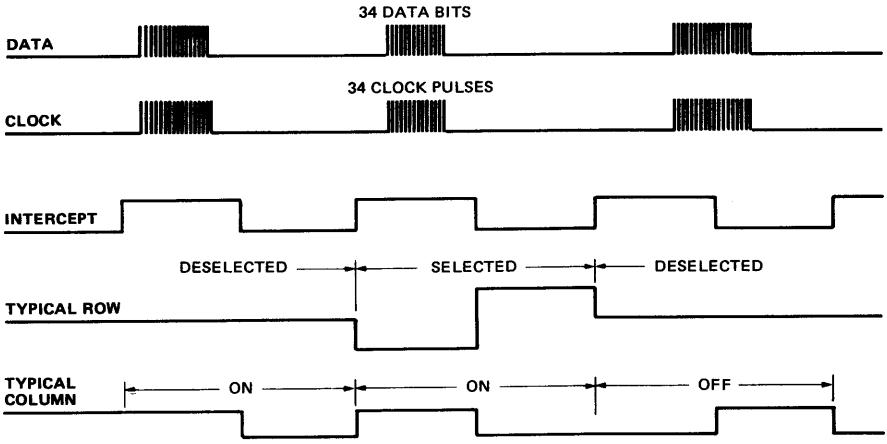
T = 25°C and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			750	μA
Input High Level	V_{IH}		.8 V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		$V_{DD}-15$	.5V_{DD}	V
Input Leakage	I_L			5	μA
Input Capacitance	C_I			5	pf
Row and Column Output Impedance	R_{on}	I_L = 10μA		40	KΩ
Interrupt Out Impedance	R_{on}	I_L = 100μA		3	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ to Interrupt Out Delay	t_D			600	nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	M
DC Offset Voltage, Any Display Element	V_{OFF}			50	mV
Row Output High	V_{OH}	Typical	V_{DD}		V
Row Output Low	V_{OL}	Typical	0		V
Row Output Unselected	V_{OM}	Typical	.5V_{DD}		V
Column Output High	V_{OH}	Typical	.68V_{DD}		V
Column Output Low	V_{OL}	Typical	.32V_{DD}		V

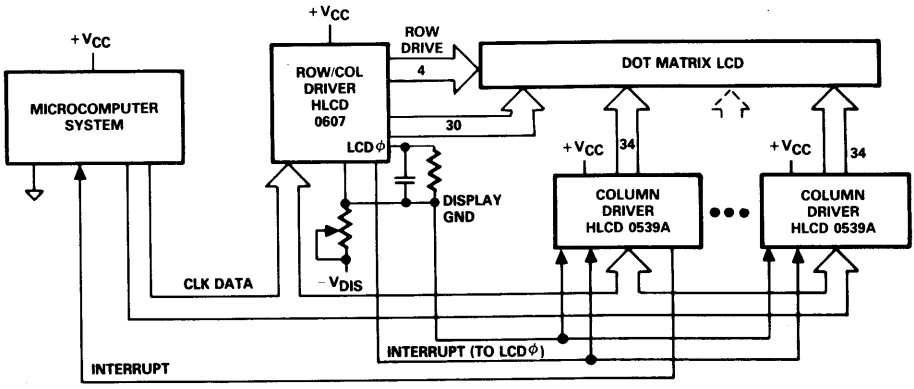
TIMING DIAGRAM



TYPICAL WAVEFORMS



TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.

2. A logic 1 on Data In causes a segment to be visible.

3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of interrupt out.

4. Row waveforms are out of phase with interrupt out if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.

5. Column waveforms are in phase with interrupt out if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.

6. The intended mode of operation is as follows:

a. Interrupt Output frequency is the minimum no flicker frequency (>30 Hz) times the number of backplanes utilized.

b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.

c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.

d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDϕ input with 50% duty cycle.

e. Backplanes are addressed sequentially and individually.

7. The LCDϕ pin can be used in two modes. If LCDϕ is driven, the Interrupt Output will follow it. LCDϕ will also oscillate if a resistor and capacitor are connected in parallel to ground. The resistor value should be at least 1MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at interrupt out.

8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDϕ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDϕ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select.

9. There are two obvious signal races to be avoided:

a. Changing data when clock is falling, and

b. Allowing Interrupt Output rising edge to be very close to clock falling edge.

10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.

11. Output locations correspond to a clockwise advancing shift register, thus R1 is the last data loaded and C30 is the first data loaded.

12. The RMS voltages this circuit delivers to individual LCD pixels depends on VDD and the number of backplanes (N) used according to the following equations:

$$V_{RMS\ OFF} = V_{DD}\sqrt{\frac{.0324\ N + .07}{N}}$$

$$V_{RMS\ ON} = V_{DD}\sqrt{\frac{.0324\ N + .43}{N}}$$

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