# M50740A-XXXSP/FP, M50741-XXXSP/FP
# M50740ASP

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

## DESCRIPTION

The M50740A-XXXSP, M50741-XXXSP and the M50740ASP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 52-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among the M50740A-XXXSP, M50741-XXXSP and the M50740ASP are noted below. The following explanations apply to the M50740A-XXXSP. Specification variations for other chips are noted accordingly.

| | |
|---|---|
| M50740A-XXXSP | ROM 3072bytes<br>Port P0, P1, P2·····Pull-up transistor option<br>Port P3·····Pull-down transistor option<br>Port R·····Input exclusive option |
| M50741-XXXSP | ROM 4096bytes |
| M50740ASP | External ROM type of M50740A-XXXSP |

The differences among the M50740A-XXXSP and the M50740A-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

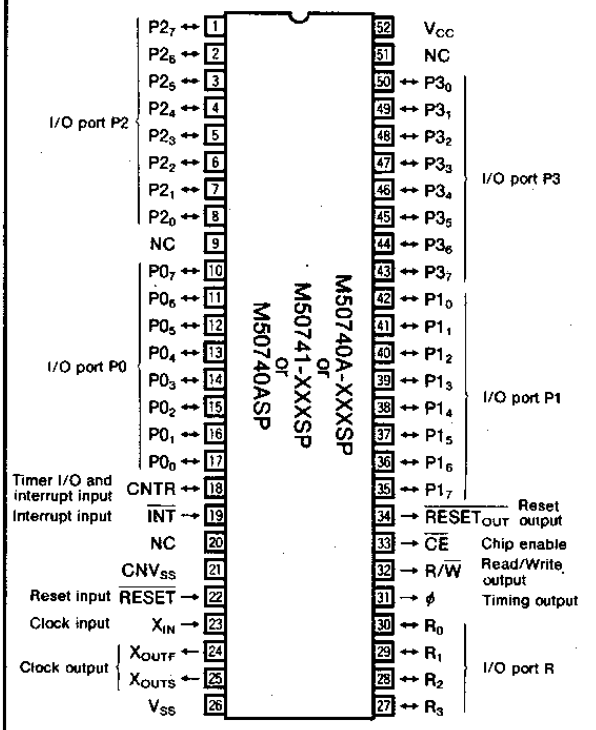
## DISTINCTIVE FEATURES

- Number of basic instructions ····· 70
- Memory size ROM ·····3072bytes (M50740A-XXXSP)
  4096bytes (M50741-XXXSP)
  RAM ····· 96bytes
- Instruction executing time
  ····· 2$\mu$s (minimum instructions at 4MHz frequency)
- Single power supply f($X_{IN}$)=4MHz ····· 5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ····· 15mW ($V_{CC}$=5V, Typ.)
- Subroutine nesting ····· 48 levels (Max.)
- Interrupt ····· 6types, 5 vecters
- 8-bit timer ····· 3
- Programmable I/O (Ports P0, P1, P2, P3) ····· 32

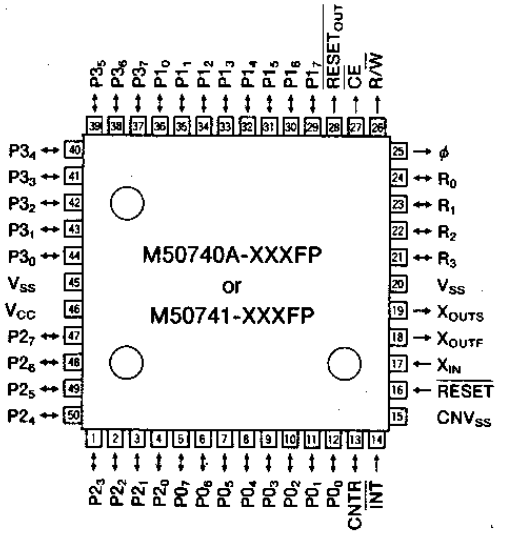
## APPLICATION

VCR, Tuner, Audio-visual equipment

## PIN CONFIGURATION (TOP VIEW)



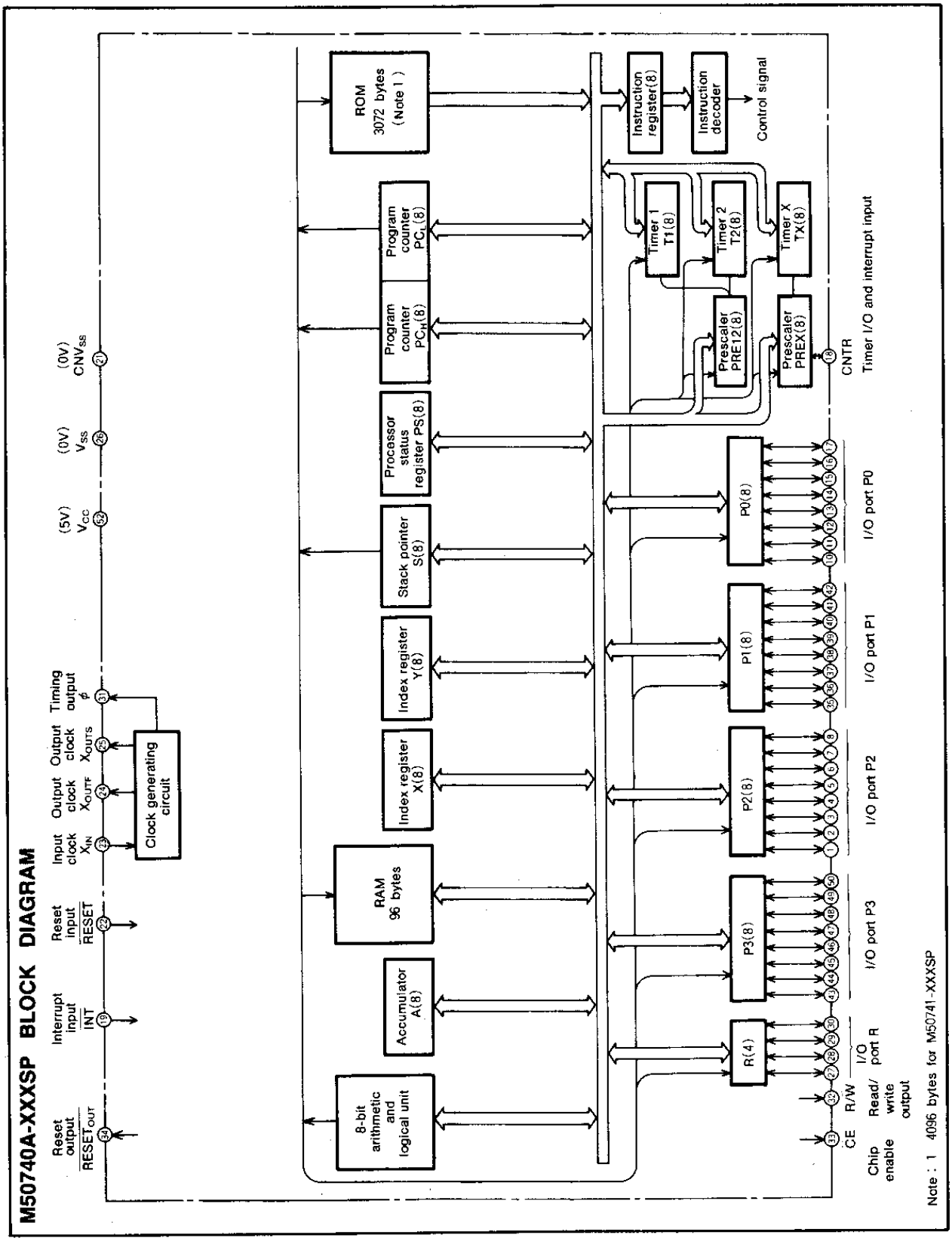

Outline 52P4B




Outline 50P6

For M50740ASP, $CNV_{SS}$ should be connected to $V_{CC}$

NC : No Connection






MITSUBISHI ELECTRIC

## FUNCTIONS OF M50740A-XXXSP

| Parameter | | | Functions |
|---|---|---|---|
| Number of basic instruction | | | 70 |
| Instruction execution time | | | 2μs (minimum instructions, at 4MHz frequency) |
| Clock frequency | | | 4MHz |
| Memory size | ROM | | 3072bytes (4096bytes for M50741-XXXSP) |
| | RAM | | 96bytes |
| I/O port | $\overline{INT}$ | Input | 1-bit×1 |
| | P0, P1, P2, P3 | I/O | 8-bit×4 |
| | R | I/O | 4-bit×1 |
| | CNTR | I/O | 1-bit×1 |
| Timers | | | 8-bit prescaler×2+8-bit timer×3 |
| Subroutine nesting | | | 48 level (max.) |
| Interrupts | | | External interrupt 2, Timer interrupt 3 |
| Clock generating circuit | | | Built-in (RC, ceramic or quartz crystal oscillator) |
| Supply voltage | at operating | | 5V±10% |
| Power dissipation | at high speed | | 15mW (at 4MHz frequency) |
| I/O characteristics | I/O voltage | | 12V (ports P0, P1, P2, $\overline{INT}$, CNTR) |
| | Output current | | 10mA (ports P0, P1, P2, P3) |
| Memory expansion | | | Possible |
| Operating temperature range | | | −10~70℃ |
| Device structure | | | CMOS silicon gate process |
| Package | M50740A-XXXSP, M50741-XXXSP, M50740ASP | | 52-pin shrink plastic molded DIP |
| | M50740A-XXXFP, M50741-XXXFP | | 50-pin plastic molded QFP |

## PIN DESCRIPTION

| Pin | Name | Input/ Output | Functions |
|---|---|---|---|
| $V_{CC}$ $V_{SS}$ | Supply voltage | | Power supply inputs 5V±10% to $V_{CC}$, and 0V to $V_{SS}$. |
| $CNV_{SS}$ | $CNV_{SS}$ | | This is usually connected to $V_{SS}$(for M50740ASP, connected to $V_{CC}$). |
| $\overline{RESET}$ | Reset input | Input | To enter the reset state, the reset input pin must be kept at a "L" for more than 2$\mu$s (under normal $V_{CC}$ conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time. |
| $X_{IN}$ | Clock input | Input | This chip has an internal clock generating circuit.<br>To control generating frequency, an external RC circuit is connected between the $X_{IN}$ and $X_{OUTS}$ or the $X_{OUTF}$ pins, and an external ceramic or a quartz crystal oscillator is connected between the $X_{IN}$ and $X_{OUTS}$ pins. If an external clock is used, the clock source should be connected to the $X_{IN}$ pin, and the $X_{OUTS}$ and $X_{OUTF}$ pins should be left open. |
| $X_{OUTS}$ | Clock output | Output | This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a RC circuit, a ceramic or a quartz crystal oscillator between this pin and $X_{IN}$ pin. |
| $X_{OUTF}$ | Clock output | Output | This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a RC circuit between this pin and $X_{IN}$ pin. |
| $\phi$ | Timing output | Output | This is the timing output pin. |
| CNTR | Timer I/O or interrupt input | I/O | This is in common with an I/O for the timer X and an interrupt input pin. |
| $\overline{INT}$ | Interrupt input | Input | This is the lowest order interrupt input pin. |
| $P0_0$~$P0_7$ | I/O port P0 | I/O | Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain. |
| $P1_0$~$P1_7$ | I/O port P1 | I/O | Port P1 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P2_0$~$P2_7$ | I/O port P2 | I/O | Port P2 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P3_0$~$P3_7$ | I/O port P3 | I/O | Port P3 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain. |
| $R_0$~$R_3$ | I/O port R | I/O | Port R is a 4-bit I/O port, and is used to connect with an I/O expander. For M50740A-XXXSP, it can be only for input. |
| R/$\overline{W}$ | Read/Write output | Output | This pin outputs read/write signal for I/O expander. |
| $\overline{CE}$ | Chip enable output | Output | This pin outputs the chip enable signal for I/O expander. |
| $\overline{RESET_{OUT}}$ | Reset output | Output | This pin outputs the reset signal for I/O expander. |

## BASIC FUNCTION BLOCKS

### MEMORY

A memory map for the M50740A-XXXSP is shown in Figure 1. Addresses $1400_{16}$ to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 3072 bytes.

Addresses $1000_{16}$ to $1FFF_{16}$ are the ROM address area assigned to the M50741-XXXSP.

Addresses $1F00_{16}$ to $1FFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $1FF4_{16}$ to $1FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses $0000_{16}$ to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses $0000_{16}$ to $005F_{16}$ are assigned to the built-in RAM and consist of 96 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

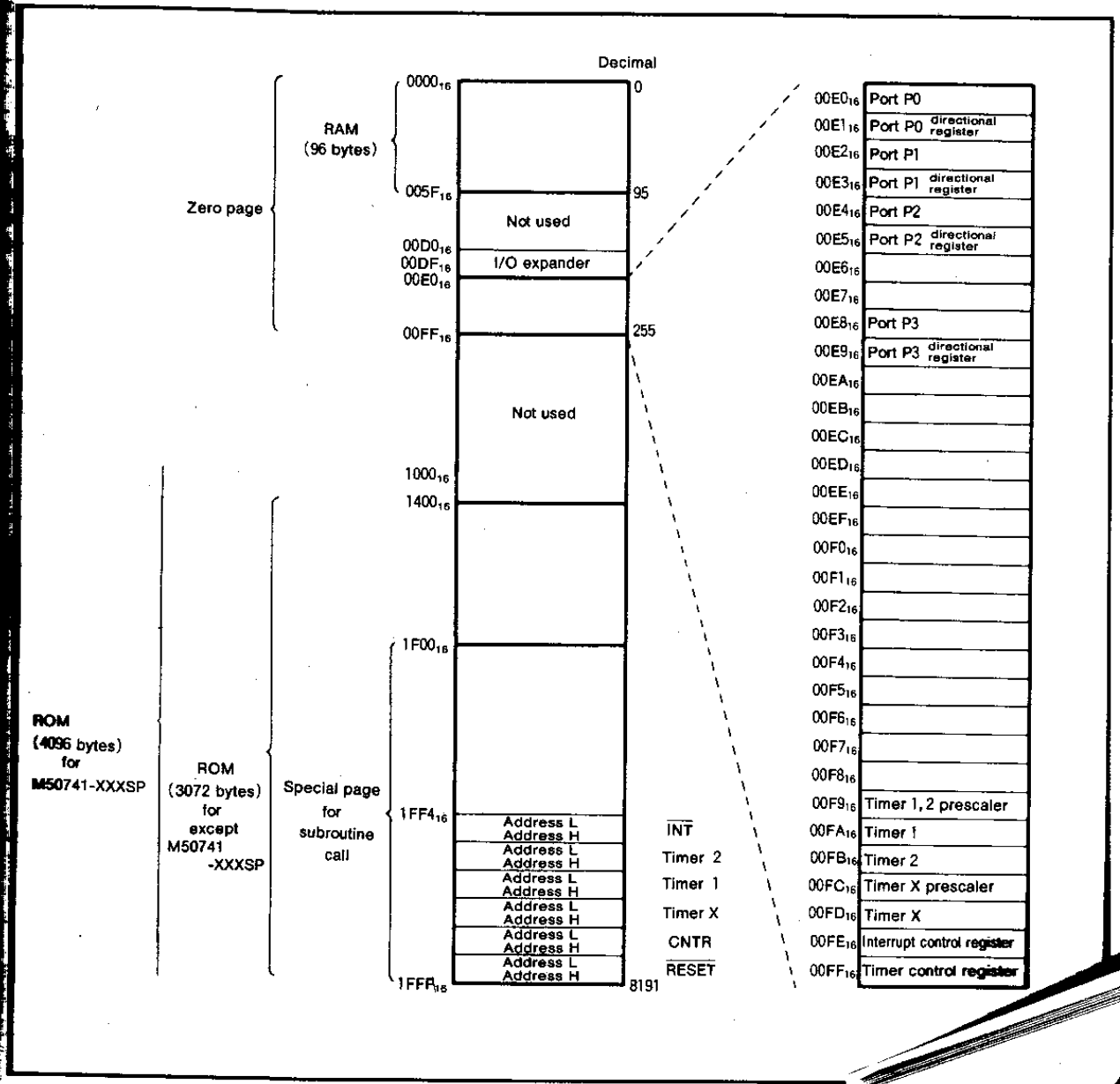



Fig.1 Memory map

## CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

## ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

## INDEX REGISTER X (X)

The index register X is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

## INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

## STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is $XX_{16}$, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

## PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers $PC_H$ and $PC_L$. The program counter is used to indicate the address of the next instruction to be executed. $PC_H$ is only 5 bits long.

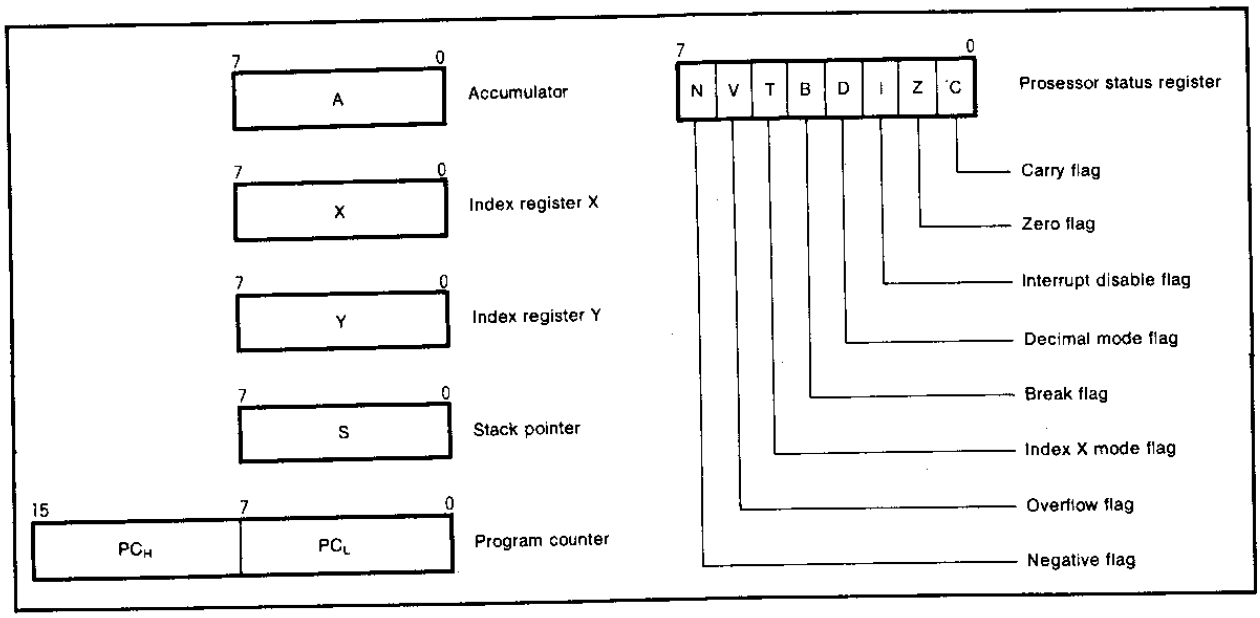



Fig.2 Register structure

## PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

### 1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

### 2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

### 3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

### 4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

### 5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

### 6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

### 7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The oveflow flag is reset by the CLV instruction and there is no set instruction.

### 8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

## INTERRUPT

The M50740A-XXXSP can be interrupted from seven souces; CNTR, timer X, timer 1, timer 2, or $\overline{INT}$/BRK instruction.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the CNTR or $\overline{INT}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT}$ generated the interrupt.

**Table 1 Interrupt vector address and priority**

| Interrupt | Priority | Vector address |
|---|---|---|
| $\overline{RESET}$ | 1 | $1FFF_{16}$, $1FFE_{16}$ |
| $\overline{CNTR}$ | 2 | $1FFD_{16}$, $1FFC_{16}$ |
| Timer X | 3 | $1FFB_{16}$, $1FFA_{16}$ |
| Timer 1 | 4 | $1FF9_{16}$, $1FF8_{16}$ |
| Timer 2 | 5 | $1FF7_{16}$, $1FF6_{16}$ |
| $\overline{INT}$(BRK) | 6 | $1FF5_{16}$, $1FF4_{16}$ |

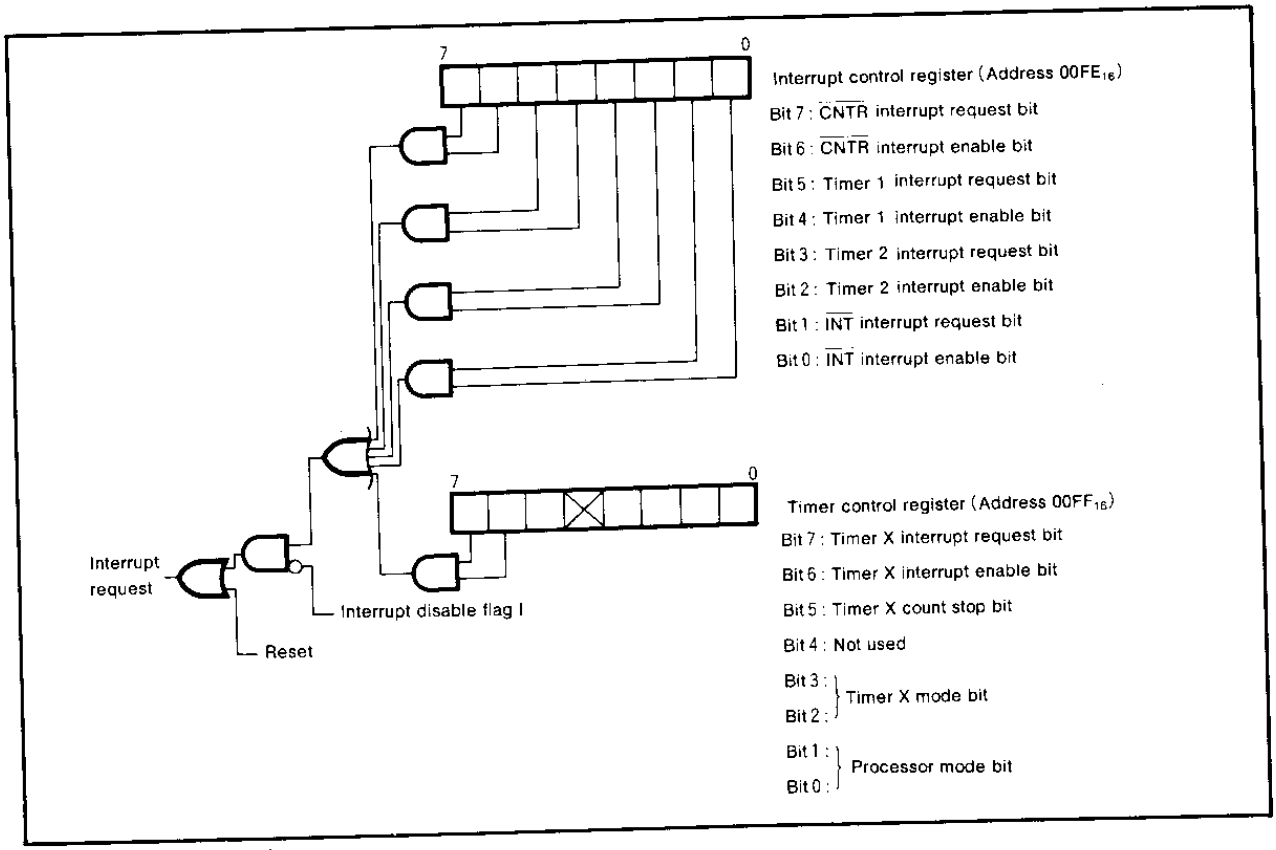



**Fig.3 Interrupt control**

## TIMER

The M50740A-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+2)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

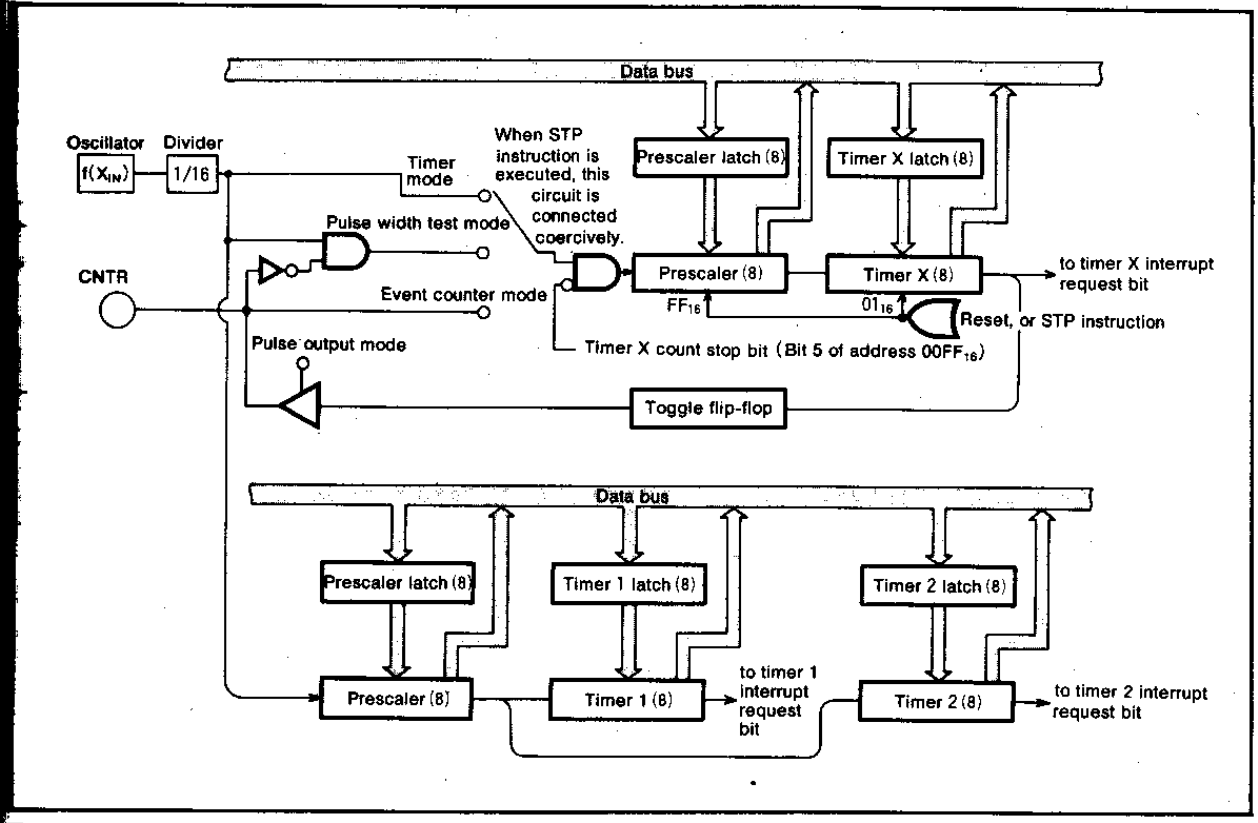



Fig.4 Block diagram of timer X, timer 1 and timer 2

(4) Pulse width measurement mode (11)

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to $FF_{16}$ and $01_{16}$, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

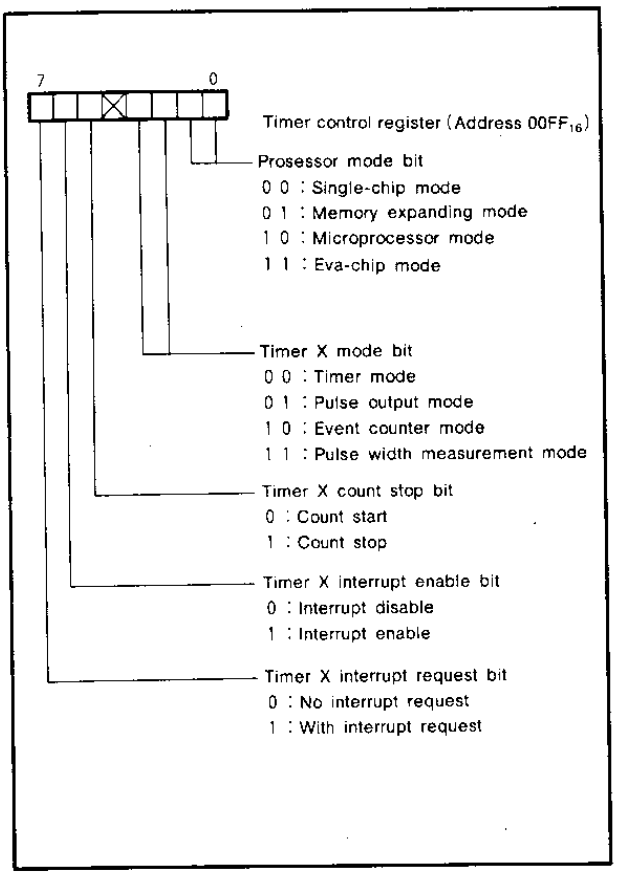



Fig.5 Structure of timer control register

| | | Address | |
|---|---|---|---|
| 1 | Port P0 directional register | ( $E1_{16}$ ) ··· | $00_{16}$ |
| 2 | Port P1 directional register | ( $E3_{16}$ ) ··· | $00_{16}$ |
| 3 | Port P2 directional register | ( $E5_{16}$ ) ··· | $00_{16}$ |
| 4 | Port P3 directional register | ( $E9_{16}$ ) ··· | $00_{16}$ |
| 5 | Prescaler X | ( $FC_{16}$ ) ··· | $FF_{16}$ |
| 6 | Timer X | ( $FD_{16}$ ) ··· | $01_{16}$ |
| 7 | Interrupt control register | ( $FE_{16}$ ) ··· | $00_{16}$ |
| 8 | Timer control register | ( $FF_{16}$ ) ··· | $00_{16}$ |
| 9 | Interrupt disable flag on processor status register | ( PS ) ··· | 1 |
| 10 | Program counter | ( $PC_H$ ) ··· | Contents of address $1FFF_{16}$ |
| | | ( $PC_L$ ) ··· | Contents of address $1FFE_{16}$ |

11 The output of oscillator is in the same state as the one after "FST" instruction execution, and is connected to $X_{OUTF}$ pin.

Fig.7 Internal state of microcomputer at reset

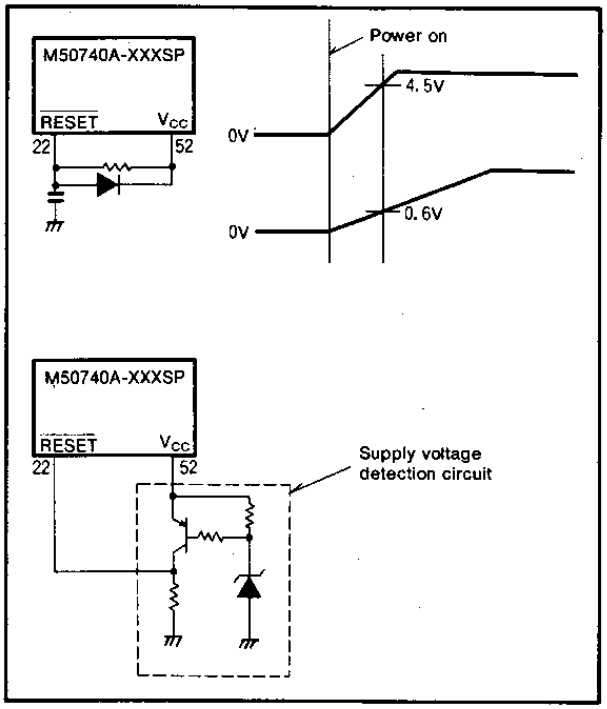



Fig.8 Example of reset circuit

## RESET CIRCUIT

The M50740A-XXXSP is reset according to the sequence shown in Figure 6. It starts the program from the address defined by the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2$\mu$s while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable, and then returned to "H" level. The internal initializations following reset are shown in Figure 7.
An example of the reset circuit is shown in Figure 8.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of $X_{IN}$-$X_{OUT}$ becomes stable.

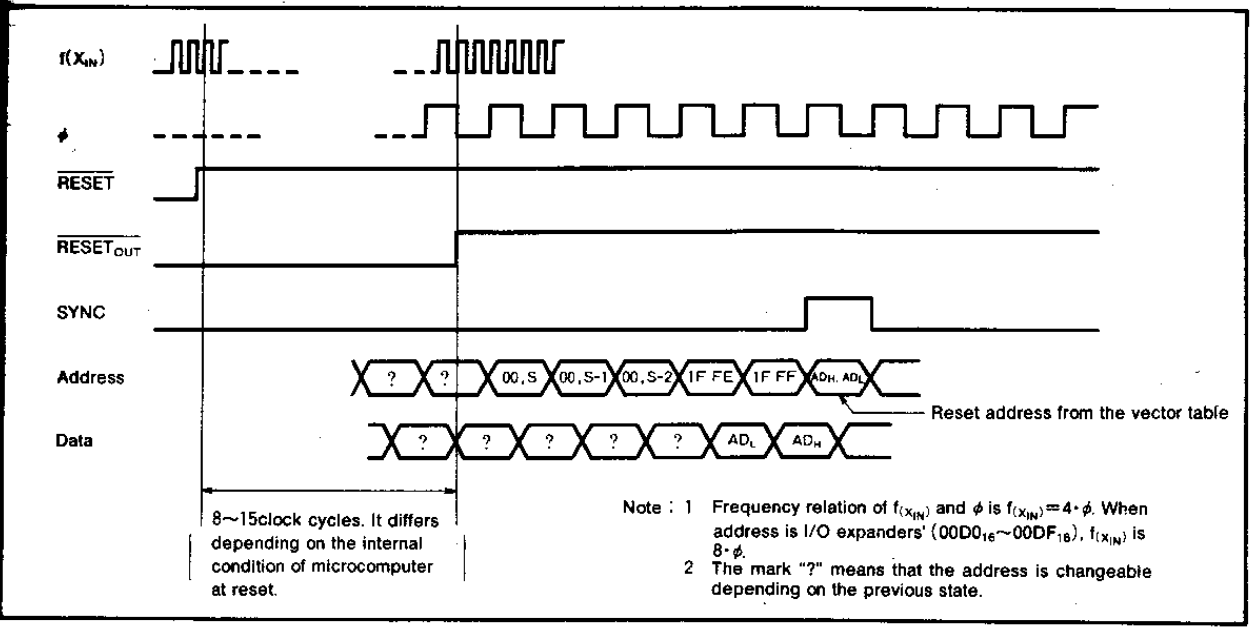



Fig.6 Timing diagram at reset

## I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

Pull-up transistor can be specified as an option for M50740A-XXXSP. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

Port P3 is an 8-bit I/O port with P-channel open drain outputs. This port also has the pull-down transistor option for M50740A-XXXSP.

(5) Port R

Port R communicates with an I/O expander. When $\phi$ goes to level "H", port R outputs the port address to that of the I/O expander. When $\phi$ goes to "L", it outputs/inputs data to from the I/O expander. The above data is effective only when $\overline{CE}$ pin goes to "L". For the M50740A-XXXSP, this port can be an input port as an option. The timing diagram is shown in Figure 9.

(6) $\overline{CE}$ pin

The $\overline{CE}$ pin goes to "L" when addresses are moved to the I/O expander addresses ($00D0_{16} \sim 00DF_{10}$). This port is used to determine whether the address or data of port R is effective.

(7) R/$\overline{W}$ pin

The R/$\overline{W}$ pin goes to "L" when the operation is executed. The R/$\overline{W}$ signal tells an external device that the CPU wants to write or read.

(8) Clock $\phi$ output pin

In normal conditions, the oscillator frequency divided by four is output as $\phi$. When $\overline{CE}$ pin goes to "L", the oscillator frequency divided by eight is output as $\phi$. This is to synchronize with I/O expander.

(9) $\overline{RESET_{OUT}}$ pin

Wne the $\overline{RESET}$ pin goes to level "L", the $\overline{RESET_{OUT}}$ pin also goes to "L". On the other hand, when the $\overline{RESET}$ pin goes to "H" the $\overline{RESET_{OUT}}$ pin also goes to "H" after 8~15 clock cycles. This output is used to reset the external devices.

(10) $\overline{INT}$ pin

The INT pin is an interrupt input pin. The $\overline{INT}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR pin

The CNTR pin is an I/O pin of timer X and also an interrupt input pin. The CNTR interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

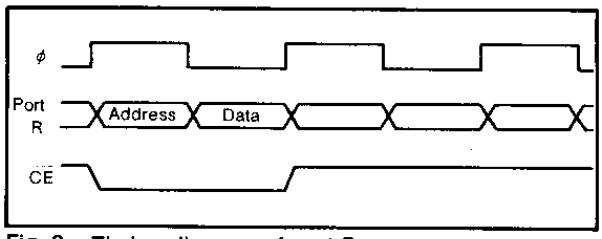



Fig. 9 Timing diagram of port R

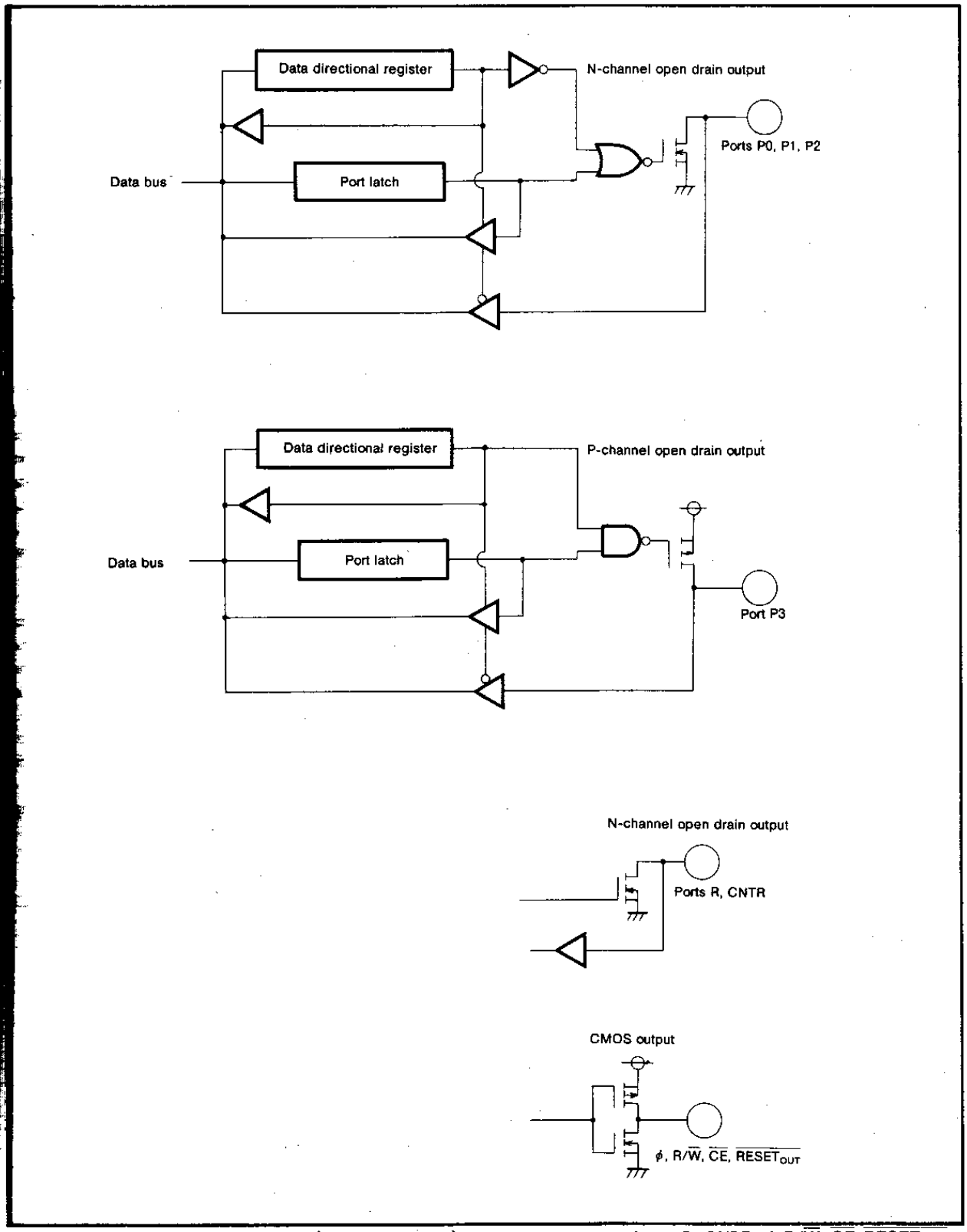



**Fig.10** Block diagram of port P0~P3 (singl-chip mode) and output formats of port R, CNTR, φ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$

## PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0 ~ P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 11 shows the functions of ports P0~P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 12.

By connecting $CNV_{SS}$ to $V_{SS}$, all four modes can be selected through software by changing the processor mode bits.

Supplying "H" level to $CNV_{SS}$ places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if $CNV_{SS}$ is connected to $V_{SS}$. Ports P0 ~ P2 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when $CNV_{SS}$ is connected to $V_{SS}$ and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when $\phi$ goes to "H" state. When $\phi$ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 5 bits of address data are output when $\phi$ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions.

Pins $P1_6$ and $P1_5$ output the SYNC and R/$\overline{W}$ control signals, respectively while $\phi$ is in the "H" state. $\overline{RDY}$ signal is input from $P1_7$. When in the "L" state, $P1_5$, $P1_6$, and $P1_7$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The $\overline{RDY}$ is a ready signal input and, when it goes to "L", internal clock stops and the CPU waits the data. However, the oscillation does not stop.

Port P2 retains its original output functions while $\phi$ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.

(3) Microprocessor mode [10]

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port $P1_5$, $P1_6$ and $P1_7$ become the R/$\overline{W}$, SYNC and $\overline{RDY}$ pins, respectively and the normal I/O functions are lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Internal memory ($00E1_{16}$ to $00E0_{16}$) cannot be used, and an external memory is needed if the address where normal I/O function have lost.

(4) Eva-chip mode [11]

When "H" level is supplied to $CNV_{SS}$ pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

With the exceptions that the internal ROM is disabled and that external memory must be attached, this mode is the same as the memory expanding mode.

The relationship between the input level of $CNV_{SS}$ and the processor mode is shown in Table 2.

**Table 2 Relationship between $CNV_{SS}$ pin input level and processor mode**

| $CNV_{SS}$ | M50741-XXXSP | | M50740A-XXXSP | | M50740ASP | |
|---|---|---|---|---|---|---|
| $V_{SS}$ | • Single-chip<br>• Memory expanding<br>• Eva-chip<br>• Microprocessor | After reset, processor mode is single chip mode.<br>All modes can be selected by changing the processor mode bit in the program. | Same as left | | — | |
| $V_{CC}$ | • Eva-chip | Eva-chip mode only | • Microprocessor<br>• Eva-chip | After reset, processor mode is microprocessor mode. Eva chip mode also can be selected by changing the processor mode bit in the program. | • Microprocessor | Microprocessor mode only. (Do not change the processor mode bit in the program). |
| +10V | — | | • Eva-chip | Eva-chip mode only | — | |

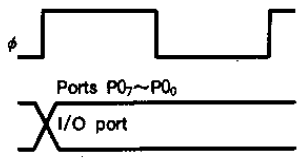
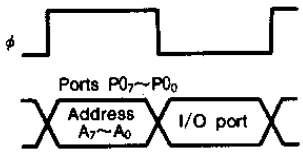
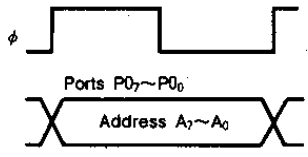
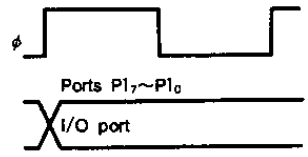
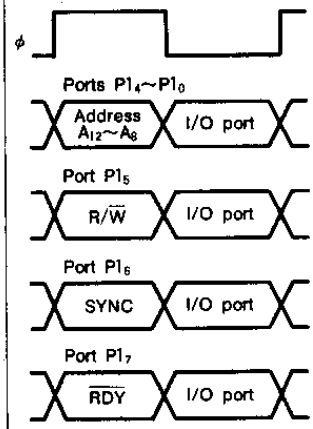
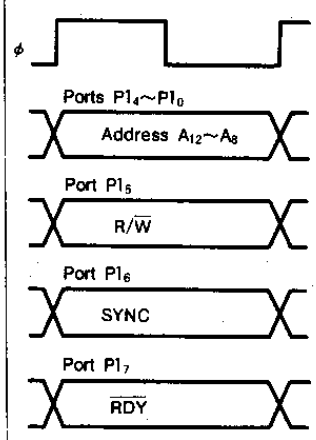
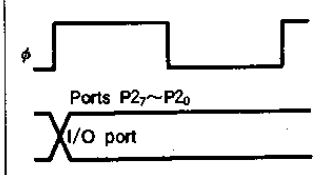
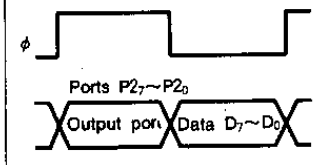
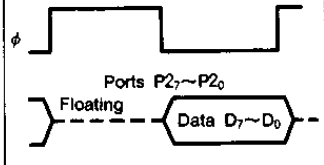
| Port \ Mode | $CM_1$ = 0, $CM_0$ = 0<br>Single-chip mode | $CM_1$ = 0, $CM_0$ = 1<br>Memory expanding mode | $CM_1$ = 1, $CM_0$ = 1<br>Eva-chip mode | $CM_1$ = 1, $CM_0$ = 0<br>Microprocessor mode |
|---|---|---|---|---|
| Port P0 |  |  | Same as left |  |
| Port P1 |  |  | Same as left |  |
| Port P2 |  |  | Same as left |  |

**Fig.11** Processor mode and functions of ports P0~P2

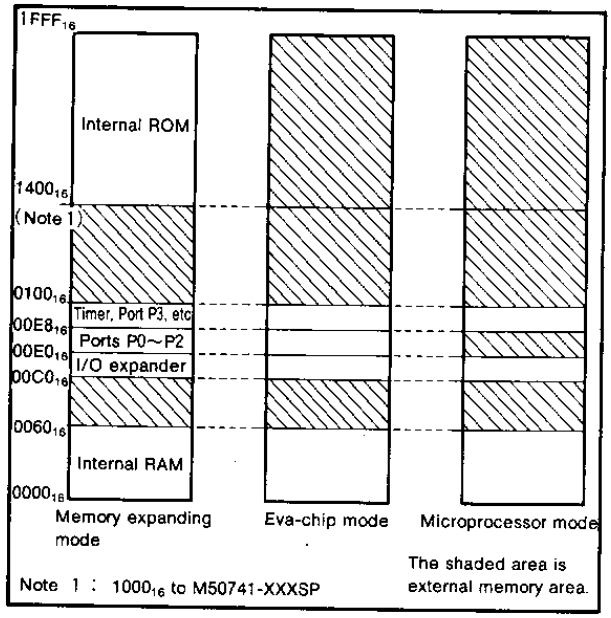



Fig.12 External memory area in processor mode

## CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 13.

When the STP instruction is executed, the oscillation of internal clock $\phi$ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with $FF_{16}$ and $01_{16}$, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock $\phi$ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

To return from the stop status, the interrupt enable bit must be set to "1" before executing STP instruction. To return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

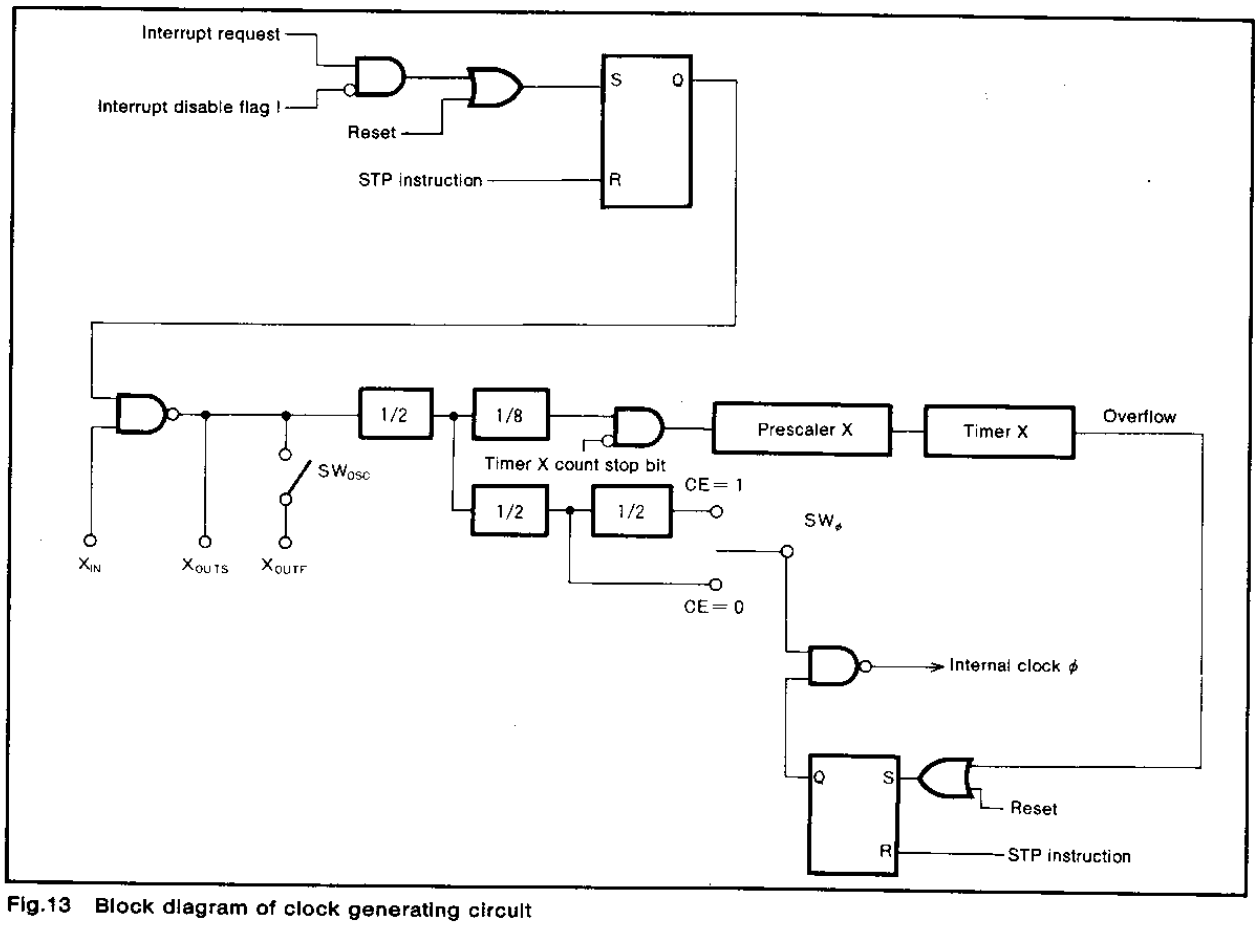



Fig.13 Block diagram of clock generating circuit



MITSUBISHI ELECTRIC

When FST instructions are executed, $SW_{OSC}$ closes and when SLW instructions are executed, it opens. These instructions are used for CR oscillation and changes oscillation frequency. The $SW_{OSC}$ closes at reset.

The $SW_\phi$ is connected to the output of oscillation frequency divided by 8 (CE=1) when addresses are I/O expanders ($00D0_{16}$~$00DF_{16}$), otherwise it is connected to the output divided by 4 (CE=0). Therefore the frequency of the internal clock $\phi$ differs depending on addresses.

This is to retain enough time for communication between I/O expander and signals.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 14.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufacturs suggested value.

The example of external clock usage is shown in Figure 15. $X_{IN}$ is the input, and $X_{OUT}$ is open.

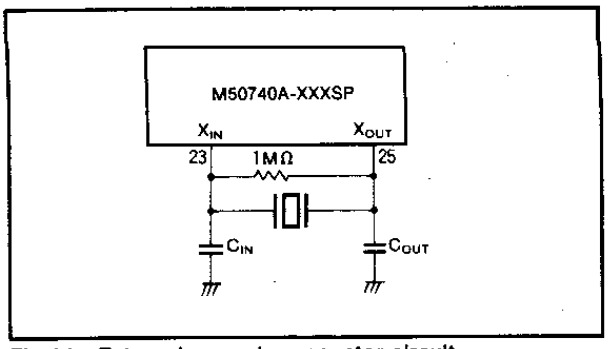



Fig.14 External ceramic resonator circuit

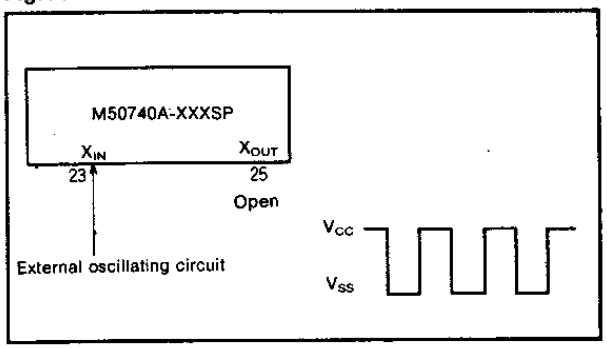



Fig.15 External clock input circuit

## PROGRAMMING NOTES

1) The frequency ratio of the timer and the prescaler is 1/(n+2).
2) Set a value other than "0" for the timer and the prescaler.
3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
4) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
6) A NOP instruction must be used after the execution of a PLP instruction.
7) The timer X and prescaler X must be set "$FF_{16}$" immediately before the execution of a STP instruction.

## DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

1) Mask ROM confirmation form
2) Mark specification form
3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port R I/O mode

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$. Output transistors cut-off. | −0.3∼7 | V |
| $V_I$ | Input voltage $R_0$∼$R_3$, $CNV_{SS}$ (Note 1), RESET, $X_{IN}$ | | −0.3∼7 | V |
| $V_I$ | Input voltage $P3_0$∼$P3_7$ | | −3.0∼$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $\overline{INT}$, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, CNTR | | −0.3∼13 | V |
| $V_O$ | Output voltage $R_0$∼$R_3$ | | −0.3∼7 | V |
| $V_O$ | Output voltage $P3_0$∼$P3_7$, $X_{OUTF}$, $X_{OUTS}$, $\phi$, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$ | | −0.3∼$V_{CC}$+0.3 | V |
| $V_O$ | Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, CNTR | | −0.3∼13 | V |
| $P_d$ | Power dissipation | $T_a$=25℃ | 1000 (Note 2) | mW |
| $T_{opr}$ | Operating temperature | | −10∼70 | ℃ |
| $T_{stg}$ | Storage temperature | | −40∼125 | ℃ |

Note 1 : −0.3∼13V for M50740A-XXXSP.
2 : 300mW for QFP types.

## RECOMMENDED OPERATING CONDITIONS ($T_a$=−10∼70℃, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Limits Min. | Limits Nom. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $V_{IH}$ | "H" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $R_0$∼$R_3$, $CNV_{SS}$ | | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage, CNTR, $\overline{INT}$ | | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage, RESET | M50740A-XXXSP, M50740ASP | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| | | M50741-XXXSP | 0.48$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage, $X_{IN}$ | | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $R_0$∼$R_3$, $CNV_{SS}$ | | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, CNTR, $\overline{INT}$ | | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $\overline{RESET}$ | | 0 | | 0.12$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $X_{IN}$ | | 0 | | 0.12$V_{CC}$ | V |
| $I_{OL(peak)}$ | "L" peak output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ | | | | 10 | mA |
| $I_{OL(avg)}$ | "L" average output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ | | | | 5 | mA |
| $I_{OH(peak)}$ | "H" peak output current, $P3_0$∼$P3_7$ | | | | −10 | mA |
| $I_{OH(avg)}$ | "H" average output current, $P3_0$∼$P3_7$ | | | | −5 | mA |
| $f_{(X_{IN})}$ | Internal clock oscillating freqency | | | | 4 | MHz |

Note 3 : High-level input voltage of up to +12V may be applied to permissible for ports P0, P1, P2, CNTR, and $\overline{INT}$
4 : The total of low-level peak output current should be 60mA max. for ports P0 and P2
The total of low-level peak output current should be 30mA max. for port P1
The total of low-level peak output current should be 80mA max. for port P3

## ELECTRICAL CHARACTERISTICS ($V_{CC}$=5V, $V_{SS}$=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | "H" output voltage, $P3_0 \sim P3_7$ | $T_a$=25℃, $I_{OH}$=−10mA | | 3 | | | V |
| $V_{OH}$ | "H" output voltage, φ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$ | $T_a$=25℃, $I_{OH}$=−2.5mA | | 3 | | | V |
| $V_{OL}$ | "L" output voltage, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $R_0 \sim R_3$, CNTR | $T_a$=25℃, $I_{OL}$=10mA | | | | 2 | V |
| $V_{OL}$ | "L" output voltage, φ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$ | $T_a$=25℃, $I_{OL}$=5mA | | | | 2 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, CNTR, $\overline{INT}$ | $T_a$=25℃ | | 0.3 | | 1 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $\overline{RESET}$ | $T_a$=25℃ | | | 0.5 | 0.7 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $X_{IN}$ | $T_a$=25℃ | | 0.1 | | 0.5 | V |
| $I_L$ | Input leak current, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $\overline{INT}$, CNTR | $T_a$=25℃, 0 ≦ $V_I$ ≦ 12V, without port option | | −12 | | 12 | μA |
| $I_L$ | Input leak current, $P3_0 \sim P3_7$, $R_0 \sim R_3$, $CNV_{SS}$, $\overline{RESET}$, $X_{IN}$ | $T_a$=25℃, 0 ≦ $V_I$ ≦ 5V, without port option | | −5 | | 5 | μA |
| $I_{IL}$ | "L" input current, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ | $T_a$=25℃, $V_I$=0V, with port option | | −60 | | −200 | μA |
| $I_{IH}$ | "H" input current, $P3_0 \sim P3_7$ | $T_a$=25℃, $V_I$=5V, with port option | | 60 | | 200 | μA |
| $V_{RAM}$ | RAM retention voltage | Stop mode | | 2 | | | V |
| $I_{CC}$ | Supply current | P-channel open drain input/output to $V_{CC}$, output terminals are opened, others to $V_{SS}$ | $f_{(X_{IN})}$=4MHz Square wave | | 3 | 6 | mA |
| | | | Stop mode $T_a$=25℃ | | | 1 | μA |
| | | | Stop mode $T_a$=70℃ | | | 10 | μA |

## TIMING REQUIREMENTS
### Single-chip mode ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $t_{su(P0D-\phi)}$ | Port P0 input setup time | 270 | | | ns |
| $t_{su(P1D-\phi)}$ | Port P1 input setup time | 270 | | | ns |
| $t_{su(P2D-\phi)}$ | Port P2 input setup time | 270 | | | ns |
| $t_{su(P3D-\phi)}$ | Port P3 input setup time | 270 | | | ns |
| $t_{su(RD-\phi)}$ | Port R input setup time | 330 | | | ns |
| $t_{h(\phi-P0D)}$ | Port P0 input hold time | 0 | | | ns |
| $t_{h(\phi-P1D)}$ | Port P1 input hold time | 0 | | | ns |
| $t_{h(\phi-P2D)}$ | Port P2 input hold time | 0 | | | ns |
| $t_{h(\phi-P3D)}$ | Port P3 input hold time | 0 | | | ns |
| $t_{h(\phi-RD)}$ | Port R input hold time | 0 | | | ns |
| $t_c$ | External clock input cycle time | 250 | | | ns |
| $t_w$ | External clock input pulse width | 75 | | | ns |
| $t_r$ | External clock rising edge time | | | 25 | ns |
| $t_f$ | External clock falling edge time | | | 25 | ns |

## Memory expanding mode and eva-chip mode

($V_{CC}$=5V±10%, Vss=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{SU(P0D-\phi)}$ | Port P0 input setup time | 270 | | | ns |
| $t_{SU(P1D-\phi)}$ | Port P1 input setup time | 270 | | | ns |
| $t_{SU(RDY-\phi)}$ | $\overline{RDY}$ input setup time | 150 | | | ns |
| $t_{SU(P2D-\phi)}$ | Port P2 input setup time | 270 | | | ns |
| $t_{h(\phi-P0D)}$ | Port P0 input hold time | 0 | | | ns |
| $t_{h(\phi-P1D)}$ | Port P1 input hold time | 0 | | | ns |
| $t_{h(\phi-RDY)}$ | $\overline{RDY}$ input hold time | 500 | | | ns |
| $t_{h(\phi-P2D)}$ | Port P2 input hold time | 0 | | | ns |

## Microprocessor mode ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{SU(\phi-RDY)}$ | $\overline{RDY}$ input setup time | 150 | | | ns |
| $t_{SU(P2D-\phi)}$ | Port P2 input setup time | 270 | | | ns |
| $t_{h(\phi-RDY)}$ | $\overline{RDY}$ input hold time | 500 | | | ns |
| $t_{h(\phi-P2D)}$ | Port P2 input hold time | 0 | | | ns |

## SWITCHING CHARACTERISTICS
## Single-chip mode ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(\phi-P0Q)}$ | Port P0 data output delay time | Fig.17 | | | 230 | ns |
| $t_{d(\phi-P1Q)}$ | Port P1 data output delay time | | | | 230 | ns |
| $t_{d(\phi-P2Q)}$ | Port P2 data output delay time | | | | 230 | ns |
| $t_{d(\phi-P3Q)}$ | Port P3 data output delay time | Fig.18 | | | 200 | ns |
| $t_{d(\phi-RA)}$ | Port R address output delay time | Fig.17 | | | 200 | ns |
| $t_{d(\phi-RAF)}$ | Port R address output delay time | | 0 | | 200 | ns |
| $t_{d(\phi-RQ)}$ | Port R data output delay time | | | | 200 | ns |
| $t_{d(\phi-RQF)}$ | Port R data output delay time | | | | 200 | ns |
| $t_{d(\phi-CE)}$ | $\overline{CE}$ output delay time | Fig.19 | | | 200 | ns |
| $t_{d(\phi-RW)}$ | R/$\overline{W}$ output delay time | | | | 100 | ns |

## Memory expanding mode and eva-chip mode

($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(\phi-P0A)}$ | Port P0 address output delay time | Fig.17 | | | 250 | ns |
| $t_{d(\phi-P0AF)}$ | Port P0 address output delay time | | | | 250 | ns |
| $t_{d(\phi-P0Q)}$ | Port P0 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P0QF)}$ | Port P0 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P1A)}$ | Port P1 address and control signal delay time | | | | 250 | ns |
| $t_{d(\phi-P1AF)}$ | Port P1 address and control signal delay time | | | | 250 | ns |
| $t_{d(\phi-P1Q)}$ | Port P1 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P1QF)}$ | Port P1 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P2Q)}$ | Port P2 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P2QF)}$ | Port P2 data output delay time | | | | 200 | ns |

## Microprocessor mode ($V_{CC}$=5V±10%, $V_{SS}$=0V, $T_a$=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(\phi-P0A)}$ | Port P0 address output delay time | Fig.17 | | | 250 | ns |
| $t_{d(\phi-P1A)}$ | Port P1 address and control signal delay time | | | | 250 | ns |
| $t_{d(\phi-P2Q)}$ | Port P2 data output delay time | | | | 200 | ns |
| $t_{d(\phi-P2QF)}$ | Port P2 data output delay time | | | | 200 | ns |

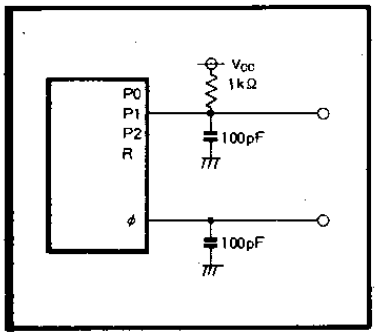



Fig.17 Ports P0~P2, R test circuit

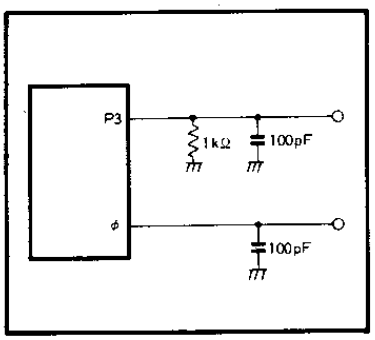



Fig.18 Port P3 test circuit

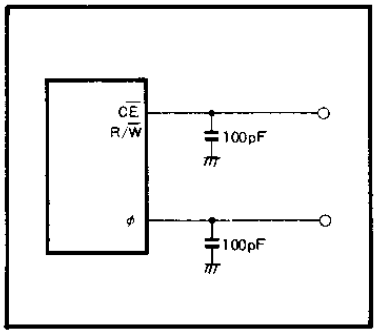
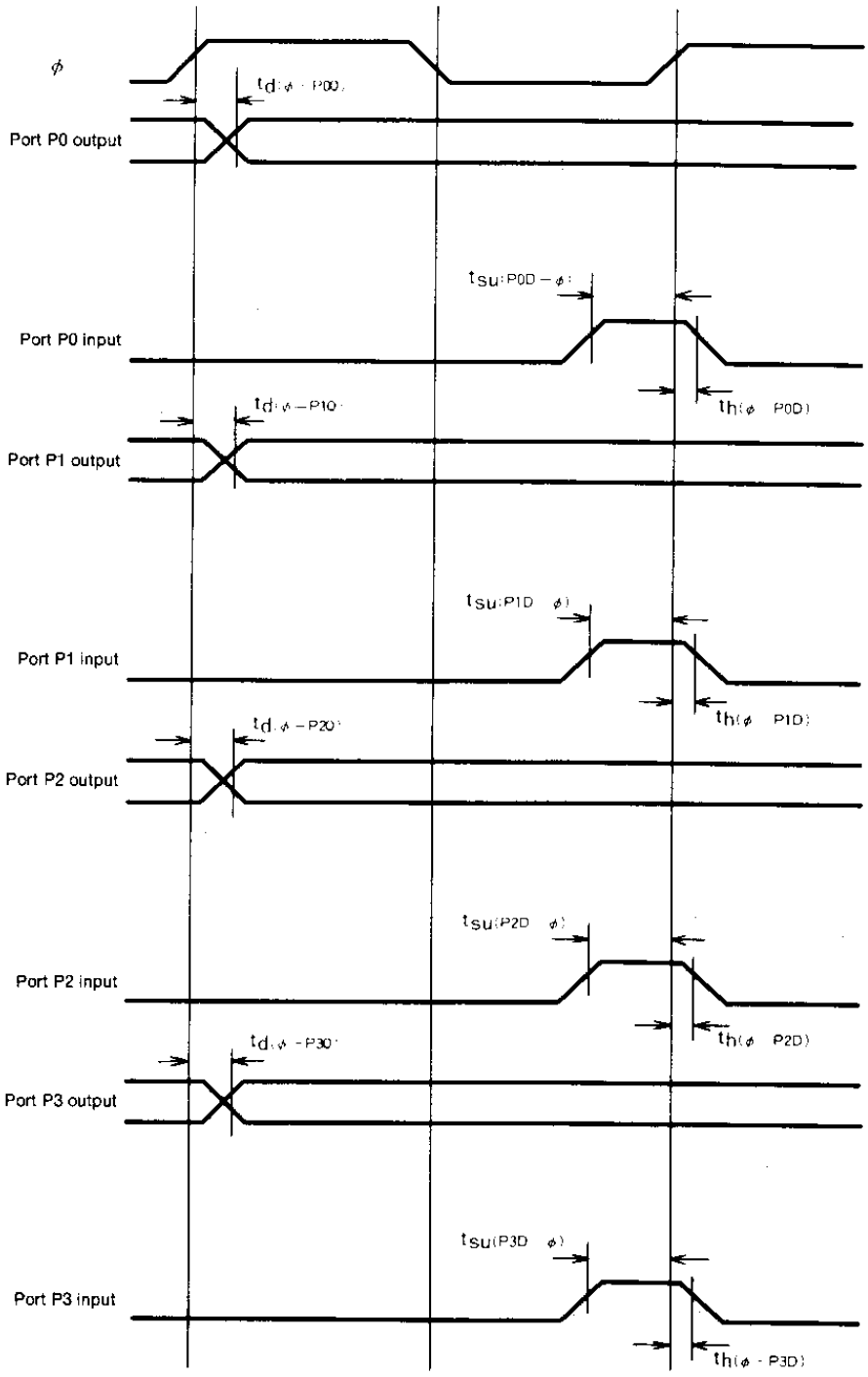


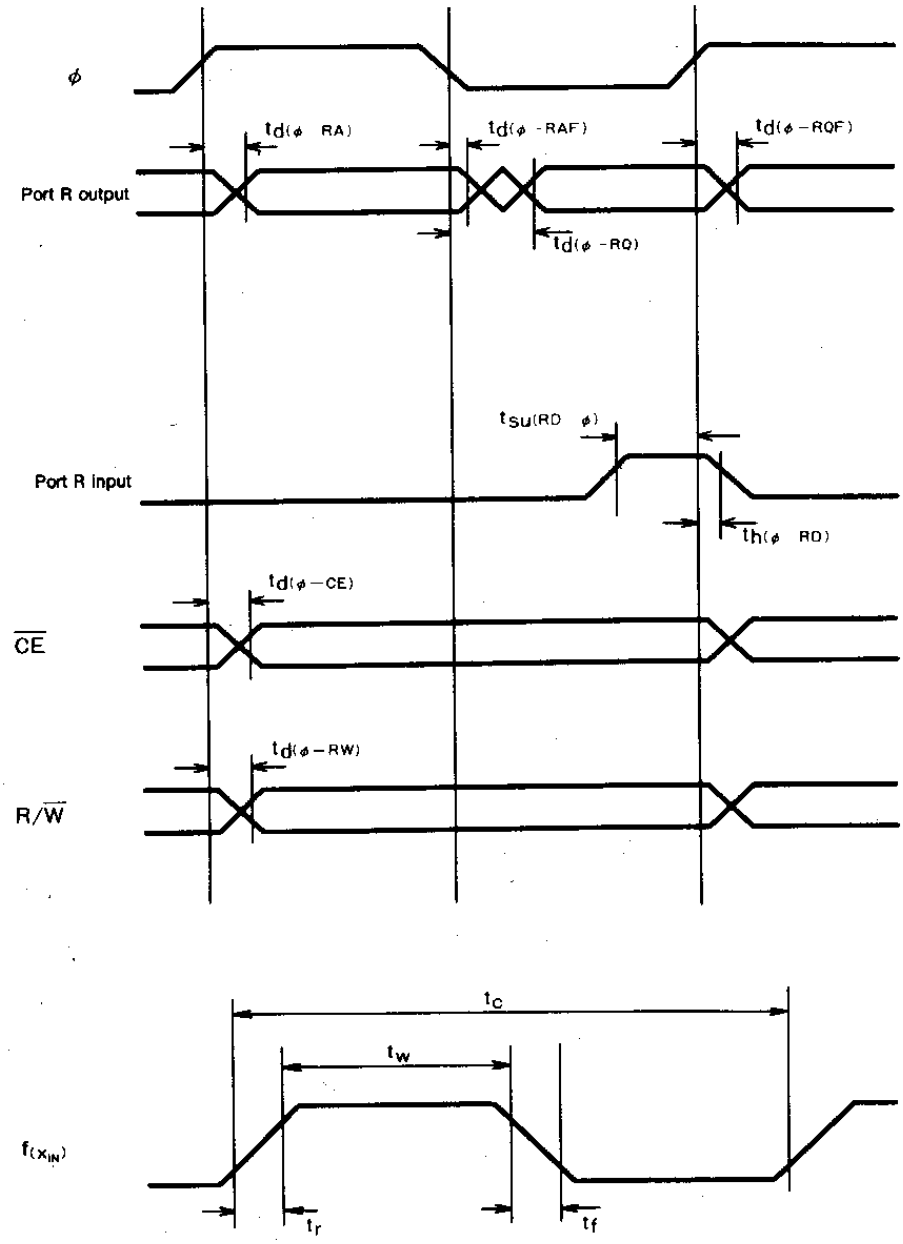

Fig.19 $\overline{CE}$ and R/$\overline{W}$ test circuit

## TIMING DIAGRAMS

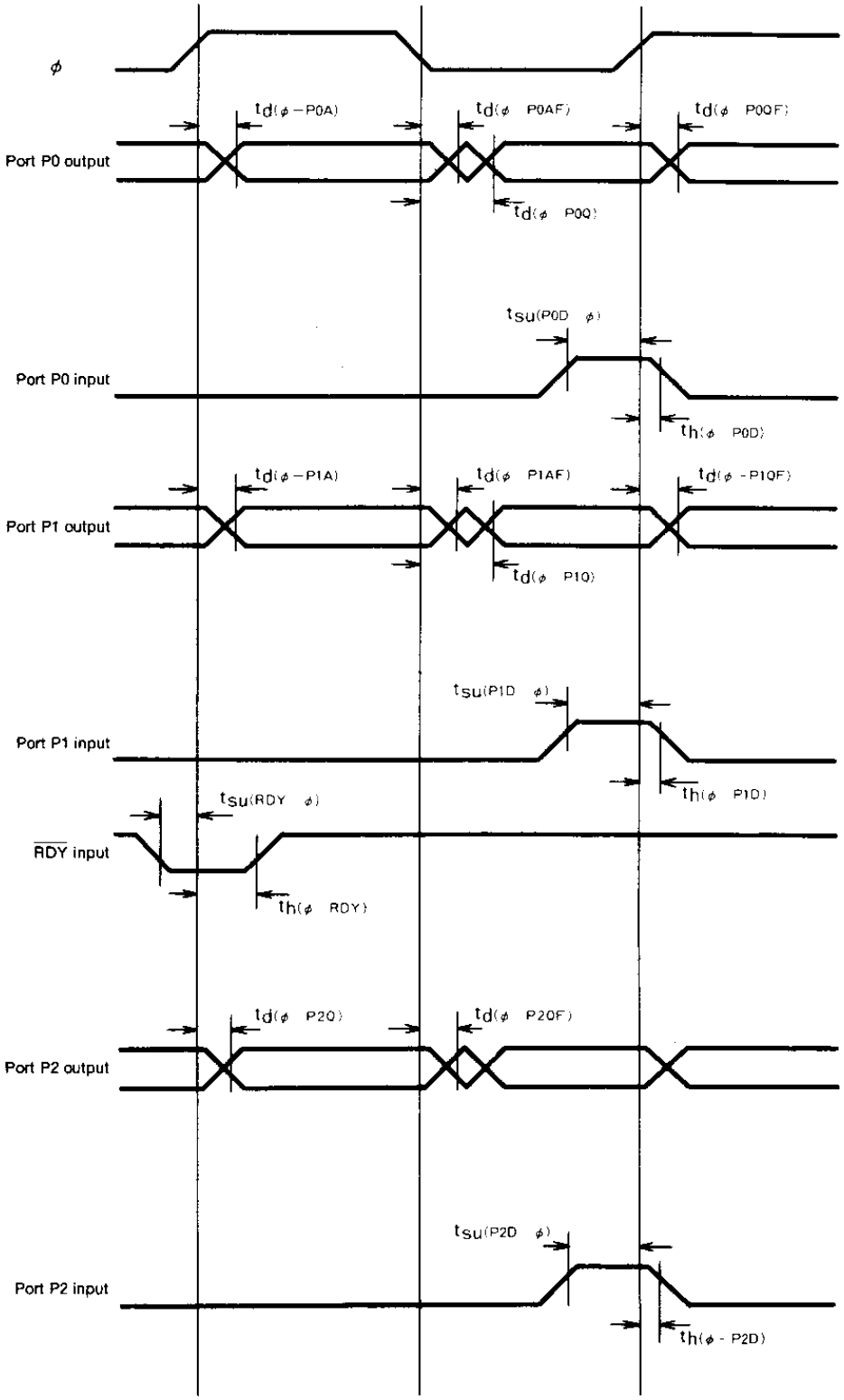
In single-chip mode



single-chip mode (continued from the preceding page)



In memory expanding mode and eva-chip mode



microprocessor mode