VIDEO AND SYSTEM CONTROLLER

GENERAL DESCRIPTION

The SCC66470B is a CMOS Video and System Controller (VSC). Integrating a high resolution bit-mapped colour display and a 680XX family system controller, the SCC66470B considerably reduces system cost.

The SCC66470B can directly drive up to 2 M bytes of memory and provides chip-select signals for both system ROM and peripherals. The on-chip DRAM controller supports up to 1 M bit (256 K x 4) DRAMs and controls access to the combined system/video DRAM. The CPU can access all memory locations even during active video display lines, thus improving system performance while reducing system cost.

FEATURES

- **Full bit-map organization**
- **Direct interface to 680XX compatible CPUs**
- **Screen resolution: up to 768 x 560 pixels**
- **4 or 8 bits per pixel**
- **Shift register for up to 15 MHz pixel rate**
- **On-chip oscillator circuitry**
- **Synchro generator for 50 and 60 Hz scan**
- **Double frequency scan**
- **Synchronization with external video**
- **1.5 M byte DRAM direct drive capability supporting up to 1 M bit (256 K x 4) DRAMs**
- **0.5 M byte ROM control**
- **1 K byte I/O control**
- **Reset sequencer and watchdog timer**
- **Fast 16-bit pixel test-and-modify logic (PIXAC)**
- **CMOS technology**
- **124-lead quad flat-pack plastic package**

APPLICATIONS

- **Home computers**
- **Personal computers**
- **Home entertainment**
- **Intelligent colour terminals**
- **Graphics, text and I/O systems**

The display resolution is programmable and between 16 and 256 colours can be selected per pixel. Studio quality pictures can be obtained by using an additional VSC which increases the number of colours to 2^{16}. The display timing is compatible with European, American and Japaneese standards for TV and TELETEXT applications.

PACKAGE OUTLINES

SCC66470B: 124-lead quad flat-pack; plastic

High-speed pixel manipulation logic (PIXAC) is provided on-chip to accelerate image manipulation (compared to software only pixel manipulation) and a coprocessor interface is provided to permit very fast manipulation of memory. The pixels are organized as PACKED PIXELS and each pixel occupies either a nibble or a byte. This allows fast test-and-modify pixel operations and pixel blitting which is much more powerful than bit blitting.

Fig. 1 shows the functional diagram and Fig. 2 shows the block diagram of the SCC66470B. The 680XX system bus is connected via 16 bidirectional data lines, 20 address lines and several control lines. Dynamic RAMS are accessed via 8 or 9 address lines (MA bus), 16 bidirectional data lines (MD bus) and control lines. The video output consists of 8 video data lines and 2 control lines. The pixel accelerator may be accessed via the system bus (by the CPU for example). It may also be accessed via the memory bus (by the coprocessor interface for example).

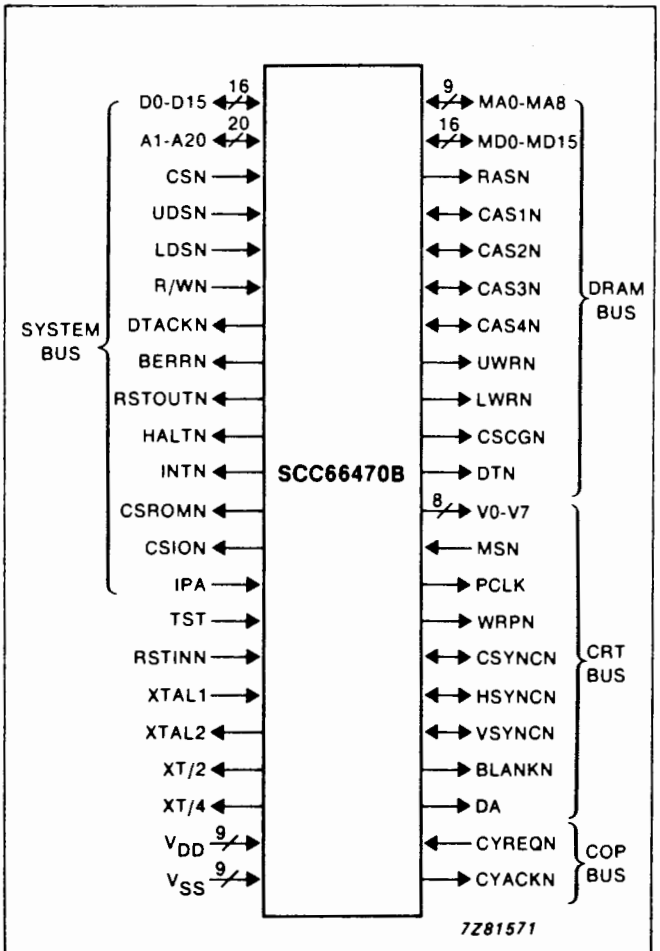


Fig. 1 Functional diagram.

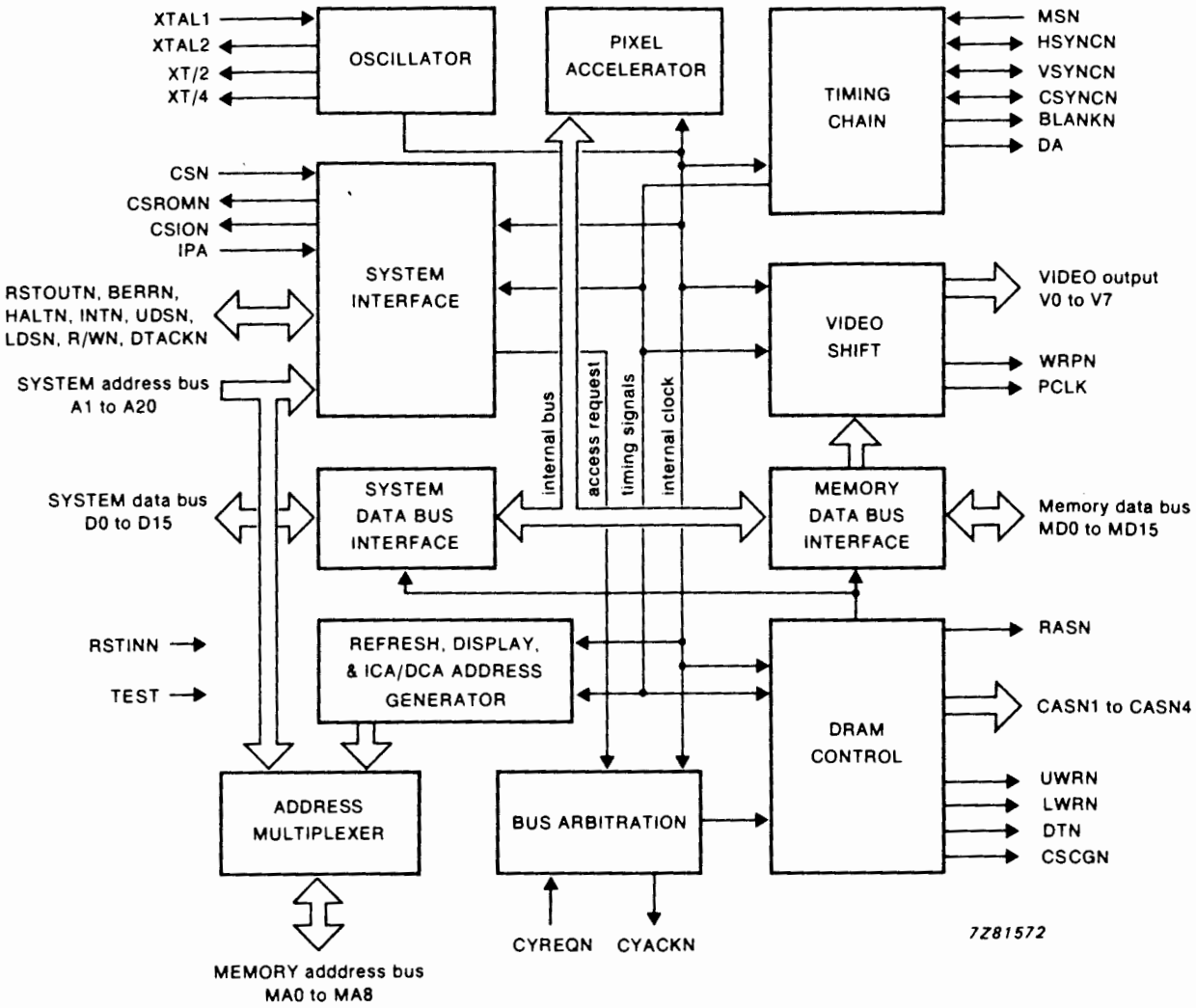


Fig. 2 Block diagram.

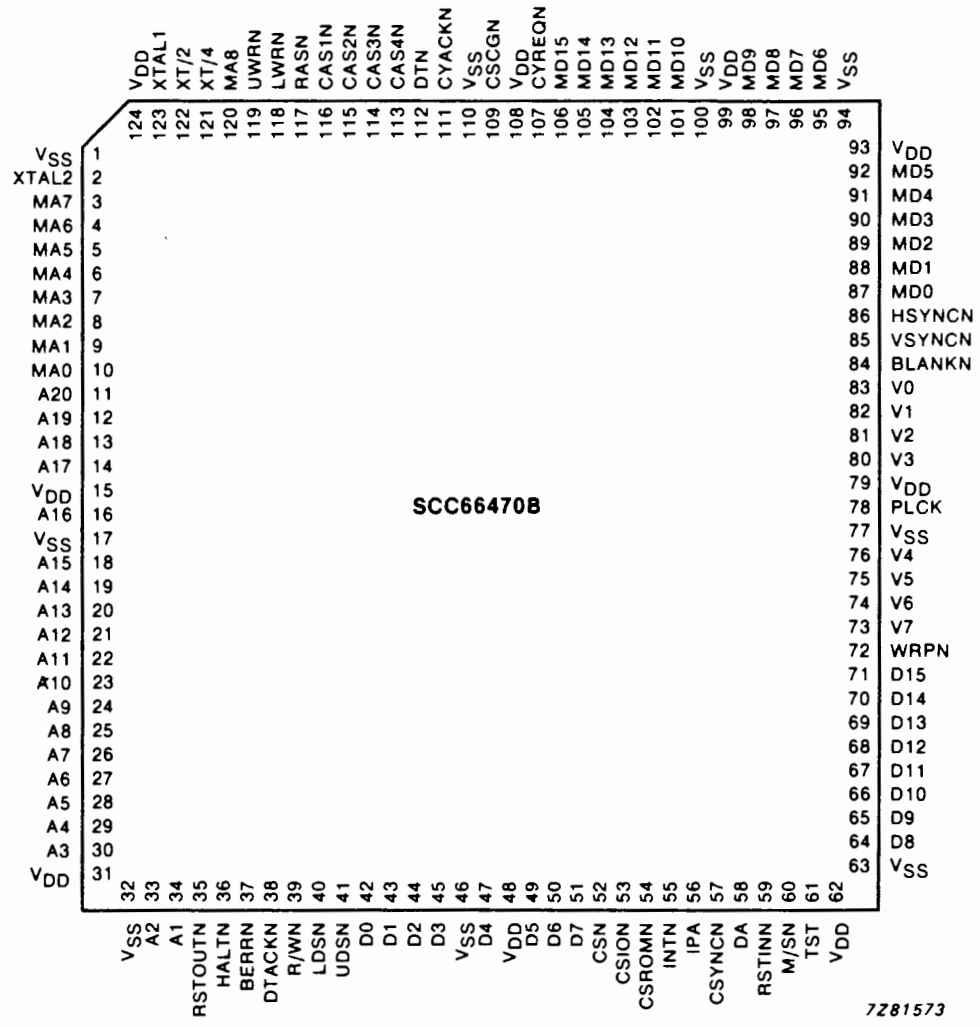


Fig. 3 Pinning diagram.

SIGNAL DESCRIPTION

mnemonic	type	pin no.	function
			System bus
A1–A20	I	11–14, 16, 18–30, 33, 34	System address bus. A1 to A20 provide the system address during system bus accesses. A1–A20 must be stable when LDSN and/or UDSN go LOW.
D0–D15	I/O	42–45, 47, 49–51, 64–71	Bidirectional 3-state data bus which is used to transfer data between the system bus and the VSC. The VSC drives the data bus during read cycles. D0–D15 must be stable when UDSN or LDSN go LOW.
UDSN	I	41	Active LOW upper data strobe. When UDSN is LOW, data on D8–D15 is being addressed.
LDSN	I	40	Active LOW lower data strobe. When LDSN is LOW, data on D0–D7 is being addressed.
R/WN	I	39	Read/write. R/WN determines the data transfer direction on the system bus. When R/WN is LOW, data is being written into VSC controlled recources.
CSN	I	52	Active LOW VSC chip select. CSN validates the address decode for system access.
DTACKN	O	38	Active LOW, 3-state data transfer acknowledge signal. DTACKN is asserted by the VSC when the system bus cycle can be continued.
RSTOUTN	O	35	Active LOW, 3-state RESET output. RSTOUTN is asserted by the VSC reset sequencer during the reset procedure.
HALTN	O	36	Active LOW, 3-state HALTN output. HALTN is asserted by the VSC reset sequencer during the reset procedure.
BERRN	O	37	Active LOW Bus Error output (3-state if programmed). BERRN is asserted by the VSC if UDSN or LDSN are still asserted at the end of the time-out period.
CSROMN	O	54	Active LOW ROM chip select. The VSC asserts CSROMN during a system bus access in the ROM address area when UDSN and/or LDSN are asserted.
CSION	O	53	Active LOW I/O chip select. The VSC asserts CSION during a system bus access in the I/O address area when UDSN and/or LDSN are asserted.
INTN	O	55	Active LOW, 3-state interrupt request output. INTN is used to generate interrupt requests to the CPU.
IPA	I	56	Active HIGH, 3-state implicit pixel accelerator addressing input. The CPU uses IPA to implicitly address the VSC pixel accelerator to increase pixel manipulation speed.

mnemonic	type	pin no.	function
			Dynamic RAM interface
MA0–MA8	I/O	3–10, 120	Memory address lines. These 3-state, multiplexed ROW/COLUMN address line outputs are used for DRAM control. Only MA0–MA7 are significant when 64 K DRAMS are used. MA0–MA8 are the least significant address input bits (A1 to A9) from a coprocessor when the CYACKN output is asserted.
MD0–MD15	I/O	87–92, 95–98, 101–106	3-state bidirectional memory data bus. MD0–MD15 also function as address and control inputs during coprocessor cycles.
RASN	O	117	Active LOW row address strobe. On the falling edge of RASN, the DRAM row address becomes valid. RASN is also used for coprocessor handshaking.
CAS1N CAS2N CAS3N CAS4N	I/O	113–116	Active LOW column address strobes for memory banks 1 to 4. On the falling edge of CASnN, the column address of memory bank n becomes valid. During the RESET period, CAS1N to CAS4N are active HIGH and validate the memory bank inputs. CAS4N is only used with 64 K devices.
CSCGN	O	109	Active LOW character ROM chip select. CSCGN is only used with the coprocessor interface.
UWRN	O	119	Active LOW upper write signal for DRAM. It is asserted when the most significant DRAM byte is being written.
LWRN	O	118	Active LOW lower write signal for DRAM. LWRN is asserted when the least significant DRAM byte is being written.
DTN	O	112	Active LOW data transfer output. DTN is used in dual port video RAM mode.
			CRT controller interface
V0–V7	O	73–76, 80–83	3-state video outputs. V0–V7 are used to output pixels and control words.
PCLK	O	78	3-state pixel clock. On the rising edge of PCLK, the video output lines (V0–V7) are valid.
WRPN	O	72	Active LOW write palette output. When WRPN is active, data available on V0–V7 is control information. WRPN is used with an external palette or a back-end chip.
VSYNCN	I/O	85	Active LOW, 3-state vertical synchronization line. In the Master mode, VSYNCN is used as a vertical synchronization output signal. In the Slave TV and Slave Dual modes, VSYNCN becomes a vertical synchronization input.
HSYNCN	I/O	86	Active LOW, 3-state horizontal synchronization line. In the Master and Slave TV modes, HSYNCN is used as a horizontal synchronization output signal. In the Slave Dual mode, HSYNC becomes a horizontal synchronization input.
CSYNCN	I/O	57	Active LOW, 3-state composite synchronization line. In the Master mode, CSYNCN generates a composite synchronization output signal. In the Slave TV mode, CSYNCN generates a symmetrical signal which generates a horizontal frequency. In the Slave Dual mode, CSYNCN generates the phase error between the master VSC and the slave VSC. When the display is disabled, the CSYNCN input is used to initialize the synchronization mode.

mnemonic	type	pin no.	function
BLANKN	O	84	Active LOW, 3-state blanking output. BLANKN is asserted during vertical and horizontal blanking periods. At all other times, it is HIGH.
DA	O	58	Active HIGH, 3-state display active output. DA is LOW during the vertical retrace period. DA is in high impedance during the horizontal retrace period and HIGH at all other times.
M/SN	I	60	Master/Slave input. The Master mode is selected when M/SN is HIGH.
			Coprocessor handshake
CYREQN	I	107	Active LOW cycle request input from coprocessor. When CYREQN is asserted, a coprocessor information transfer cycle is provoked.
CYACKN	O	111	Active LOW cycle acknowledge output to the coprocessor. CYACKN is used for coprocessor handshaking.
			Miscellaneous signals
XTAL1	I	123	Crystal oscillator input. XTAL1 may also be used to input an external clock signal.
XTAL2	O	2	Crystal oscillator output.
RSTINN	I	59	Active LOW Schmitt trigger RESET input. RSTINN is used to initiate a reset sequence and is pulled HIGH by an internal 30 kΩ pull-up resistor.
XT/2	O	122	Xtal/2 clock output. Output frequency = $f_{OSC}/2$
XT/4	O	121	Xtal/4 clock output. Output frequency = $f_{OSC}/4$
TST	I	61	Test input. TST should be tied to V_{SS} for normal operation.

Notes

1. All pins are TTL compatible except for XTAL1, XTAL2 and RSTINN which are CMOS compatible.
2. There are nine V_{DD} and nine V_{SS} pins. The following pins must be tied to V_{DD}: 15, 31, 48, 62, 79, 93, 99, 108, 124; the following pins must be tied to V_{SS}: 1, 17, 32, 46, 63, 77, 94, 100, 110.

FUNCTIONAL DESCRIPTION

The SCC66470B performs the following functions:

A. **System Control:** Integrates the necessary logic for a minimal system.

B. **Dynamic RAM Control:** Direct drive for several types of DRAM.

C. **Display Control:** On-chip timing chain, video address generator and shift register. A special reload mechanism permits the use of dynamic control words during display.

D. **Pixel Manipulation:** On-chip logic optimized for image manipulation.

E. **Coprocessor Interface:** On-chip interface which enables the SCC66470B to be used with a coprocessor or CPU.

A. SYSTEM CONTROL

The VSC performs the following 680XX system control functions:

Reset and Halt Operations

The SCC66470B is reset when the RSTINN pin is released. The timing chain then counts 8 video frames before the HALTN and RSTOUTN are simultaneously released.

Memory Swapping

After RSTINN is released, the VSC routes the first four 680XX accesses to the ROM (CSN must be asserted). After swapping, the ROM is decoded normally (180000H).

Address Decoding

The VSC is connected to the system bus via 20 address lines. Thus, 2 M bytes (each word = 2 bytes) may be accessed via the VSC. Memory mapping depends on the type of DRAM used (64 K or 256 K) and on the synchronization mode (see Table 1).

DTACKN Generation

The SCC66470B generates the Data Acknowledge signal as follows:

- Access to DRAM is acknowledged as soon as it is certain that data will be available for the CPU. DTACKN can be advanced by two clock periods using the ED bit in the CSR register.
- Access to internal registers is acknowledged immediatly after arbitration against a potential access from the coprocessor.
- Access to system ROM is ackowledged after approximately 16 clock periods. DTACKN will be advanced by 8 clock periods if the DD bit in the CSR register is set. This gives a maximum DTACKN delay of either 350 ns or 600 ns with a 30 MHz crystal.
- Access to system I/O devices (CSION pin) is acknowledged by the addressed device and not by the VSC.
- Access to DRAM I/O (CCSION) is acknowledged in the same way as access to DRAM. The device is considered synchronous with accesses on the memory data bus.

Bus Error Generation

The BERRN signal is asserted when the BE bit in the Control register CSR is set and when the selection is not acknowledged for at least one complete video line (approximately 64 μs). The BE flag bit is then set in CSR. When the CPU reads the CSR status register, the BERRN pin and the BE flag are reset.

Interrupt Generation

The VSC generates interrupt requests to the CPU by asserting the INTN pin. The following conditions can generate an interrupt:

- The Dynamic Control Mechanism (DCA) fetches an interrupt instruction. Then, the IT1 bit of the CSR register is set.
- The pixel accelerator (PIXAC) code is reset by the coprocessor. Then, the IT2 bit of the CSR register is set.

The INTN pin, IT1 and IT2 are reset when the CPU reads the CSR register.

B. DRAM INTERFACE

The SCC66470B has an on-chip Dynamic RAM controller which may be programmed for normal, page, nibble and video RAM devices.

Driving Modes

The VSC can directly drive up to 16 memory devices. They may be arranged in one bank of 16 devices (64 K x 1 or 256 K x 1 DRAMS) on in several banks of four devices (64 K x 4 or 256 K x 4 DRAMS). The TD bit in the CSR register selects either 64 K or 256 K DRAMS.

DRAM Access and Arbitration

The DRAM can be used as system memory and video memory. Thus, the CPU or coprocessor can access any portion of the entire memory space during active video display time. The DRAM can also be accessed by several masters and on-chip arbitration logic is implemented to provide each master with a guaranteed access time (timing window). The various masters are:

- The system bus (CPU or DMA cycles)
- The display
- ICA/DCA controller
- The DRAM refresh controller
- The coprocessor bus.

Table 1 Address Map

	256 K		64 K	
ADDRESS	MASTER OR SLAVE TV	SLAVE DUAL	MASTER OR SLAVE TV	SLAVE DUAL
000000 01FFFF	BANK 1	BANK1	BANK 1	
020000 03FFFF			BANK 2	
040000 05FFFF			BANK 3	
060000 07FFFF			BANK 4	
080000 09FFFF	BANK 2	BANK 2		BANK 1
0A0000 0BFFFF				BANK 2
0C0000 0DFFFF				BANK 3
0E0000 0FFFFF				BANK 4
100000 17FFFF	BANK 3	BANK 3		
180000 1FFBFF	SYSTEM ROM		SYSTEM ROM	
1FFC00 1FFF7F	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O
1FFF80 1FFFBF	DRAM I/O		DRAM I/O	
1FFFC0 1FFFDF		INTERNAL REGISTERS		INTERNAL REGISTERS
1FFFE0 1FFFFF	INTERNAL REGISTERS		INTERNAL REGISTERS	

DRAM access cycles contain pairs of timing windows. Each cycle has a duration of 16 XTAL periods. The first window is used by video related functions (Display or ICA/DCA controllers) and the DRAM refresh controller. The second window is available for DRAM accesses from the system bus (CPU or DMA cycles) or from the coprocessor bus. When the video and refresh functions are inactive, DRAM accesses are free-running with no windows so that a system or coprocessor access can occur at any time and the appropriate RASN and CASN signals are asserted.

Fig. 4 shows the number of cycles related to the time domain of a complete video frame. Note that:

- RF1 and RF2 are refresh cycles
- ICA and DCA only exist when they are enabled
- RF2 only exists in the LOGICAL SCREEN mode
- If the display is not enabled, all areas other than the refresh areas are FREE-RUN
- In Dual-port mode, all display windows other than the first display window of each line (1 window) are available to the system bus.

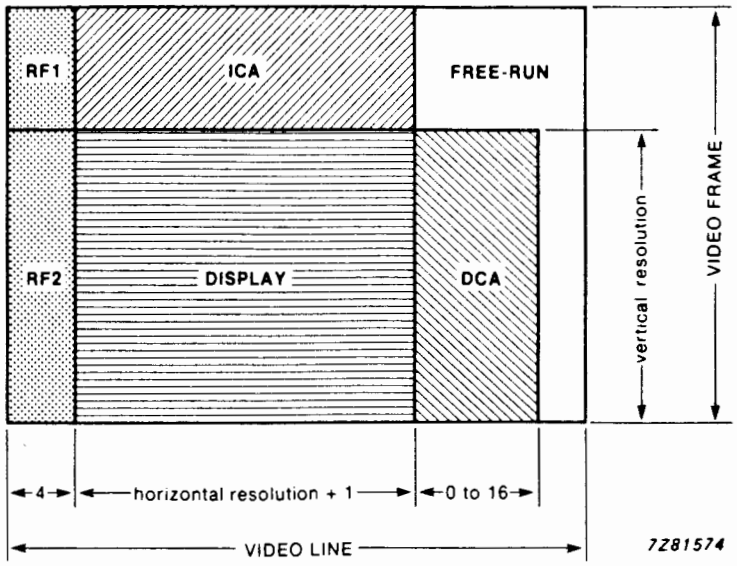


Fig. 4 DRAM cycles.

DRAM Timing

The SCC66470B can use normal, nibble, page or dual-port video DRAM types. Two bits in the CSR register (DM1 and DM2) are used to select the DRAM type. In the page and nibble modes, DRAM timing is in the FAST mode. In the FAST mode, two display fetches are performed in the same cycle. In the nibble mode, the LSB and MSB address lines may be switched externally. In the dual port video RAM mode, the CPU has twice as much access time available during the display window and the DTN output is asserted at the beginning of each video line. Fig. 5 shows cycle windows in the display area in both the SLOW and FAST modes.

DRAM Deselect

During a RESET, a memory bank will be deselected if its corresponding CASN pin is grounded and no DTACKN will be generated for this bank. To select the memory bank, a pull-up resistor is required.

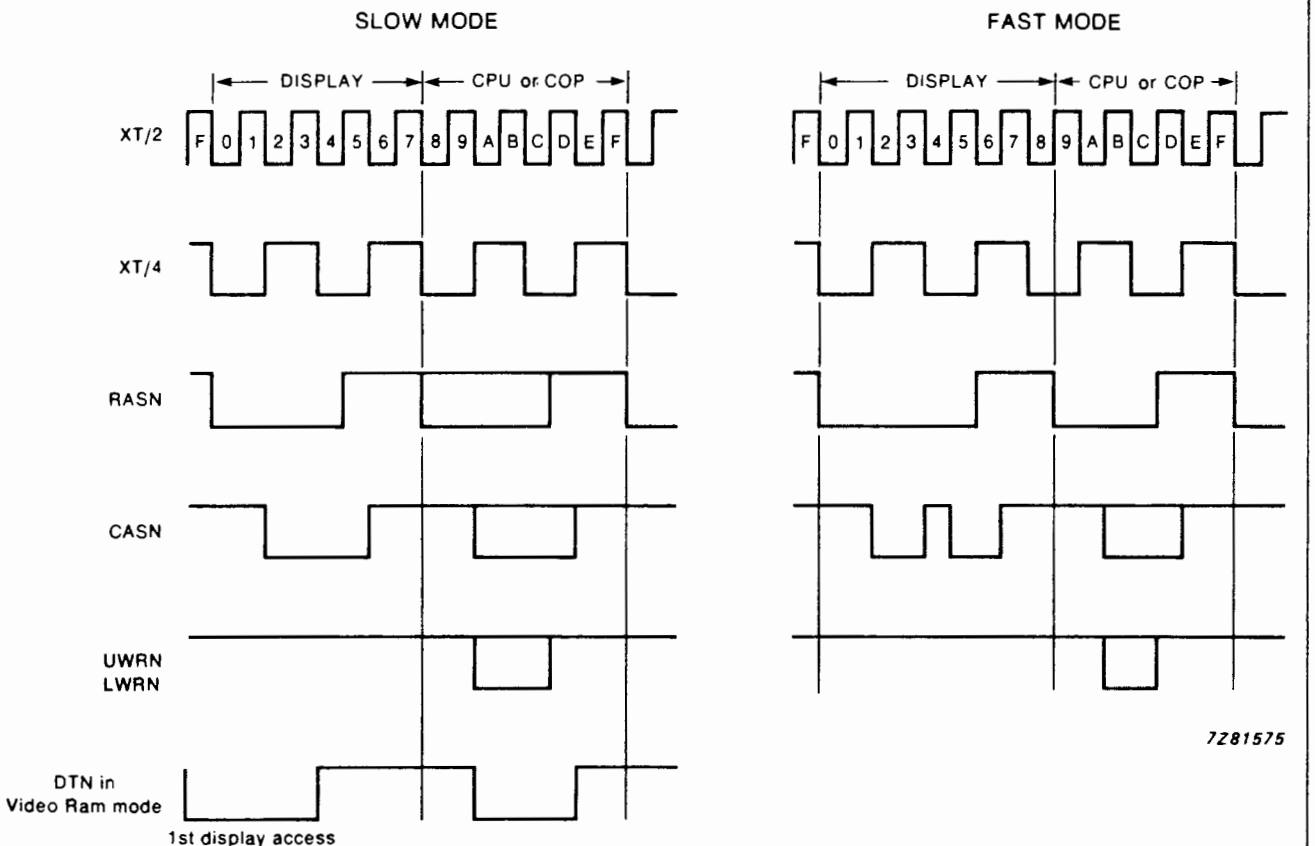


Fig. 5 DRAM timing.

C. DISPLAY CONTROL

Several pre-programmed display modes may be selected and the VSC contains a Video Start address register to locate the video display within the first 1 M Byte of the DRAM address space. The display logic reads a word from the video display area and then serializes it either nibble by nibble (4 bits per pixel) or byte by byte (8 bits per pixel).

Resolution

Horizontal resolution

Table 2 shows the horizontal resolution as set by bits CF1, CF2, SS and CM in the DCR register for the FAST mode (set by bits DM1 and DM2 in the CSR register). If the SLOW mode is selected or if the Double Frequency mode is active, then the horizontal resolution shown in Table 2 is halved.

Vertical resolution

Table 3 shows the vertical resolution as set by bits FD and SS in the DCR register for non-interlaced and interlaced field repeat modes. For double frequency and normal interlaced modes, the vertical resolution shown in Table 3 is doubled.

Reduced and Full Screens

In the Full Screen mode (SS = 1), the picture covers the entire TV screen. In the Reduced Screen mode (SS = 0), a border of the programmable colour is displayed on the top, bottom, left and right parts of the visible screen. The border colour register (BCR) is 8 bits wide. In the 8 bits per pixel mode, 256 colours are possible and, in the 4 bits per pixel mode, 16 colours are possible.

Physical and Logical Screen

The SCC6470B can organize the display memory in either of two ways: logical screen mode or physical screen mode. The logical screen mode is selected when the LS bit of the DCR register is set and the physical screen mode is selected when LS is reset. The Video Start Register (VSR) points to the beginning of the physical display.

In the logical screen mode, the bit map width is 512 bytes. The 9 least significant bits of the VSR register are reloaded to the beginning of each display line. A horizontal wrap-around will occur if the VSR points too far to the right of a memory line.

In the physical screen mode, the memory line width and the bit map width are the same as the display line width. The first pixel of a line immediately follows the last pixel of the previous line. In the physical screen mode, interlacing is not permitted and dual-port video RAM can not be accessed. With a 27.5 MHz oscillator, in full screen mode, the bit map is 384 pixels wide even if the display is 360 pixels wide.

Image Control Area (ICA) and Dynamic Control Area (DCA) Mechanisms.

The SCC66470B enables control information to be fetched during vertical and horizontal retrace periods. This feature is enabled via the IC and DC bits in the DCR register. The VSR register is used as a dynamic ICA/DCA pointer.

ICA Mechanisms

This mechanism consists of fetching Long Word instructions during the vertical retrace period. The ICA pointer is either 400H or 80400H at the beginning of the vertical retrace period (see Table 4). At least 500 instructions can be fetched in the ICA.

DCA Mechanism

In this case, the instruction fetch occurs during the horizontal retrace period. The DCA is located next to the display memory (see Fig. 6). In the physical screen mode, the bit map width is thus increased by the number of possible DCA fetches (see Table 5).

The number of possible fetches depends on the mode (see Table 5). This number is halved for the SLOW mode.

Screen Management

Screens and Sub Screens

The VSR register points to a display line in the 1 M Byte display RAM area. During the execution of a reload VSR instruction, the VSR register functions as an ICA/DCA pointer. The reload VSR and STOP instruction stops the ICA/DCA mechanism and facilitates a new screen (ICA) or subscreen (DCA). This permits vertical rolling and vertical split screens.

Horizontal rolling

The 2 least significant bits of the VSR should be logic 0 since the 20 bit video start address (held in VSR and the four least significant bits of the DCR register) must be Long Word aligned. However, in the logical, reduced screen and fast modes, horizontal byte rolling in screen or subscreen is possible by using these 2 VSR bits to specify a 2 byte offset.

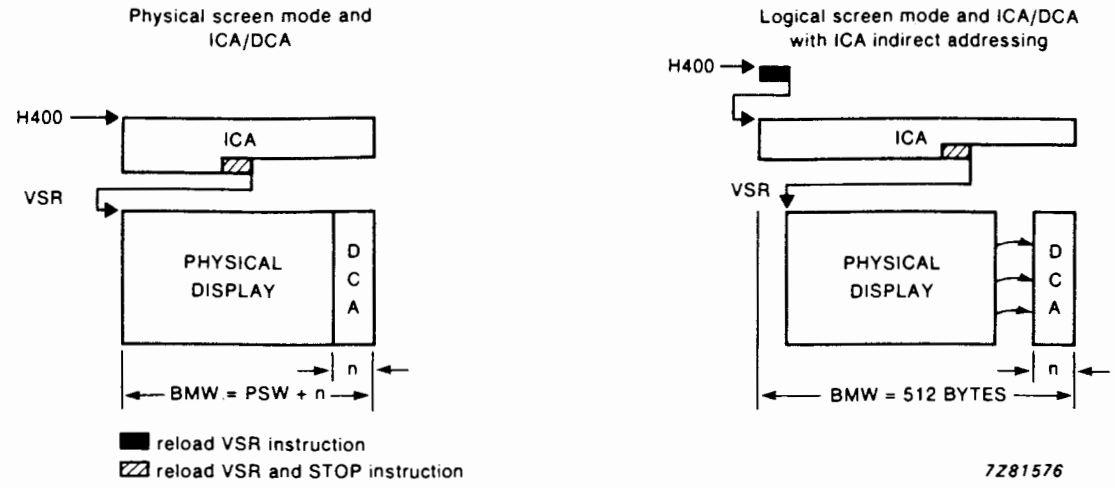


Fig. 6 ICA/DCA and physical display.

Notes to Fig. 6:

1. BMW: Bit Map Width.
2. PSW: Physical Display Width.
3. n: The DCA width is 16 or 64 in the logical screen mode. In the physical screen mode, the DCA width is 16, 32 or 64.

Table 2 Horizontal resolution

CF1	CF2	SS	f_{OSC} (MHz)	number of pixels/line CM = 1	number of pixels/line CM = 0	active line (μs)
0	0	0	19.6608	448	224	45.6
0	0	1	19.6608	512	256	52
0	1	0	24	512	256	42.6
0	1	1	24	640	320	53.3
1	0	0	27.5	640	320	46.5
1	0	1	27.5	720	360	52.4
1	1	0	30	640	320	42.6
1	1	1	30	768	384	51.2

Table 3 Vertical resolution

FD 0	SS 0	number of lines	frame duration (ms)	image frequency (Hz)
0	0	250	16	50
0	1	280	16	50
1	0	210	13.4	60
1	1	240	15.3	60

Table 4 ICA pointer

	256 K		64 K	
	bank 1 enabled	bank 1 disabled	master	slave dual
ICA pointer	H400	H80400	H400	H80400

Table 5 Number of DCA fetches

IC	DC	double frequency $\overline{SM}$.DF	SS	CF1	CF2	DCA (in bytes)
X	0	X	X	X	X	0
0	1	X	X	X	X	16 (reduced DCA mode)
1	1	1	X	X	X	16
1	1	0	0	X	X	64
1	1	0	1	0	X	32
1	1	0	1	1	0	32
1	1	0	1	1	1	64

Note: ICA/DCA instructions are Long Word Aligned and Long Word Wide. In the SLOW mode, the number of fetches is halved. X = don't care.

Table 6 ICA/DCA instruction list

code	instruction	description
00XX XXXX XXXX XXXX XXXX XXXX XXXX XXXX	STOP	Stop the control sequence. The instruction fetches are then stopped.
0100 XXXX XXXX PPPP PPPP PPPP PPPP PPPP	RELOAD VSR	Reload the VSR and the video address counter with the specified pointer. The following fetches will use the new value. The VSR is considered as an ICA or DCA pointer.
0101 XXXX XXXX PPPP PPPP PPPP PPPP PPPP	RELOAD VSR and STOP	Reload the VSR with the specified pointer and then stop the control fetches.
0110 XXXX XXXX XXXX XXXX XXXX XXXX XXXX	INTERRUPT	Generate an interrupt request to the CPU and set CSR bit, IT1.
0111 XXXX CCCC CCCC XXXX XXXX XXXX XXXX	RELOAD BORDER	Reload border colour register with specified colour immediately.
1BBB BBBB BBBB BBBB BBBB BBBB BBBB BBBB	BEP CONTROL	Back-End Processor control. The WRPN signal goes LOW. The 32 bits are passed via the video output port (V7 – V0) to the BEP without alteration. The information is always output in groups of 8 bits (equivalent to the 8 bits per pixel mode).

Notes to Table 6:

1. X = don't care.
2. P = ICA/DCA pointer data.
3. C = border colour data.
4. B = Back-End Processor information.

Pixel Output

The internal shift register outputs pixels as follows:
Memory word, MD15 - MD0 (15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0), is serialized to either:

15, 14, 13, 12, 11, 10, 9, 8 and then 7, 6, 5, 4, 3, 2, 1, 0 (8 bits per pixel) or

15, 14, 13, 12 and then 11, 10, 9, 8, then 7, 6, 5, 4, then 3, 2, 1, 0 (4 bits per pixel).

Table 7 shows the number of bits per pixel for various PCLK frequencies. If the BLANKN pin is reset (retrace period) and if WRPN is inactive, the pixel port is forced to logic 0.

Table 7 PCLK frequency and the number of bits per pixel

WRPN	CM	timing mode	bits/pixel	PCLK frequency
1	0	fast	8	XTAL/4
1	1	fast	4	XTAL/2
1	X	slow	4	XTAL/4
0	X	fast	8	XTAL/4
0	X	slow	8	XTAL/8

X = don't care.

Video Synchronization

The SCC66470B can operate in the following modes:

- Master mode: HSYNCN and VSYNCN are both outputs
- Slave TV mode: HSYNCN is an output and VSYNCN is an input
- Slave Dual mode: HSYNCN and VSYNCN are both inputs.

The VSC is initialized when the DE bit in the DCR register is reset via the CSYNCN and MSN pins.

Table 8 Synchronization

MSN	CSYNCN pin (DE = 0)	synchronization mode
1	X	Master
0	1 (no pull down)	Slave TV
0	0 (10 kΩ pull down)	Slave Dual

X = don't care.

Figures 7(a), 7(b), 8 and 9 show the HSYNCN, CSYNCN, BLANKN and DA timing in the Master and reduced screen modes.

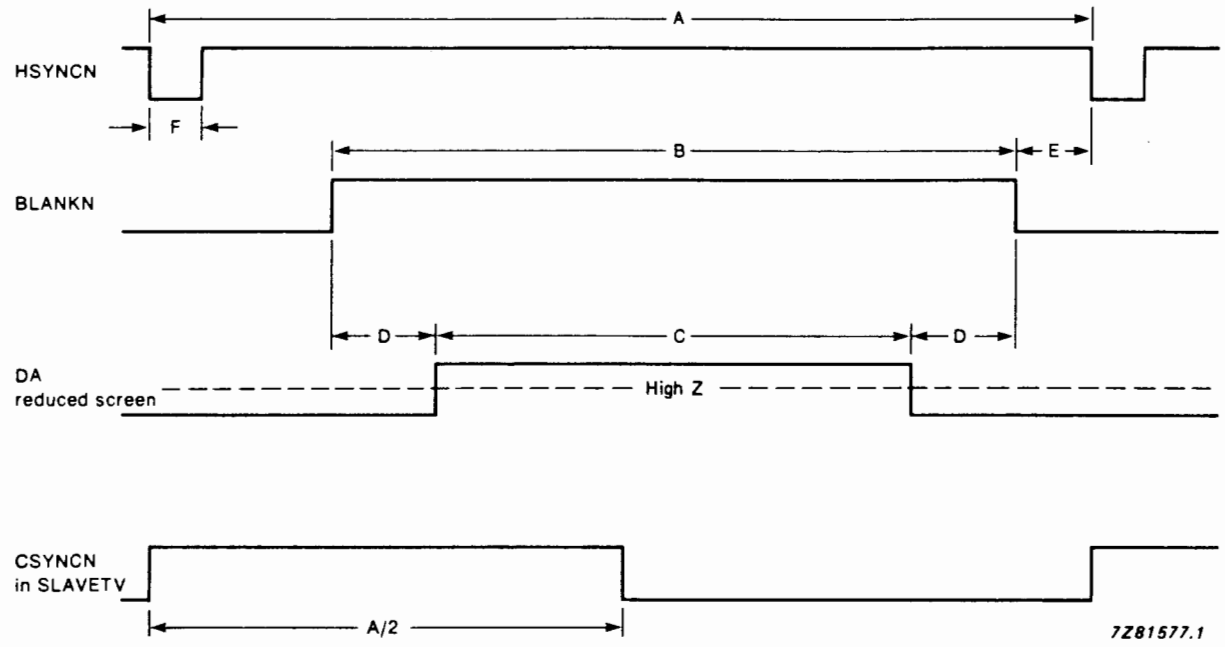


Fig. 7(a) Horizontal synchronization timing.

Table 9 Horizontal synchronization timing

	19.6608 MHz		24 MHz		27.5 MHz		30 MHz	
	cycles	µs	cycles	µs	cycles	µs	cycles	µs
A	80	65.1	96	64	110	64	120	64
B	64	52.08	80	53.33	90	52.36	96	51.2
C	56	45.47	64	42.67	80	46.55	80	42.67
D	4	3.26	8	5.33	5	2.91	8	4.27
E	2	1.63	1	0.67	2	1.16	3	1.6
F	6	4.88	7	4.67	8	4.65	9	4.8
G	3	2.44	3	2	4	2.33	4	2.13
H	6	4.88	7	4.67	8	4.65	9	4.8

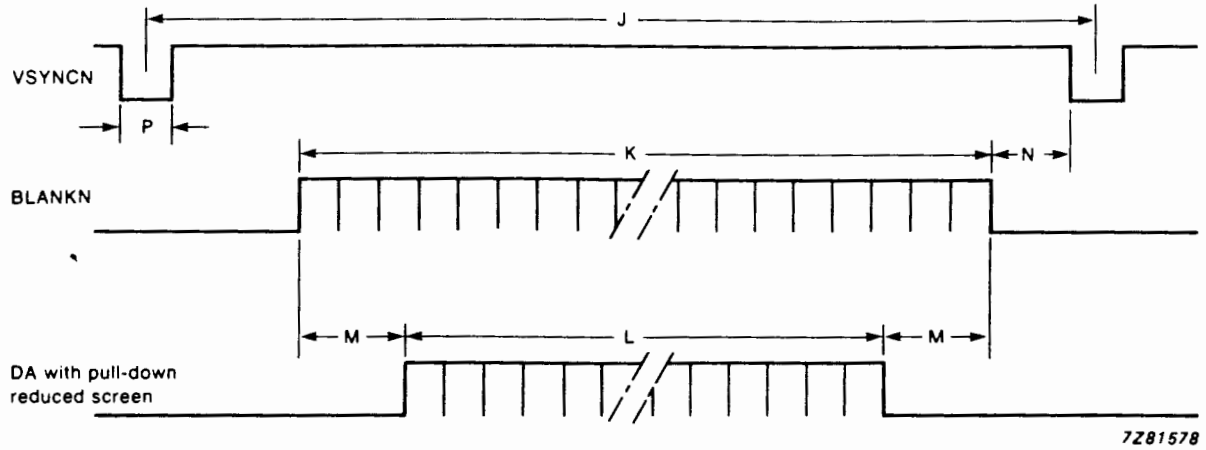


Fig. 7(b) Vertical synchronization timing.

Table 10 Vertical synchronization timing

	50 Hz non interlace		50 Hz interlace		60 Hz non interlace		60 Hz interlace	
	lines	ms	lines	ms	lines	ms	lines	ms
J	312	19.97	312.5	20	262	16.77	262.5	16.8
K	280	17.92	280	17.92	240	15.36	240	15.36
L	250	16	250	16	210	12.44	210	13.44
M	15	0.96	15	0.96	15	0.96	15	0.96
N	6	0.384	6 or 6.5	0.416	4	0.256	4 or 4.5	0.288
P	2.5	0.16	2.5	0.16	3	0.192	3	0.192

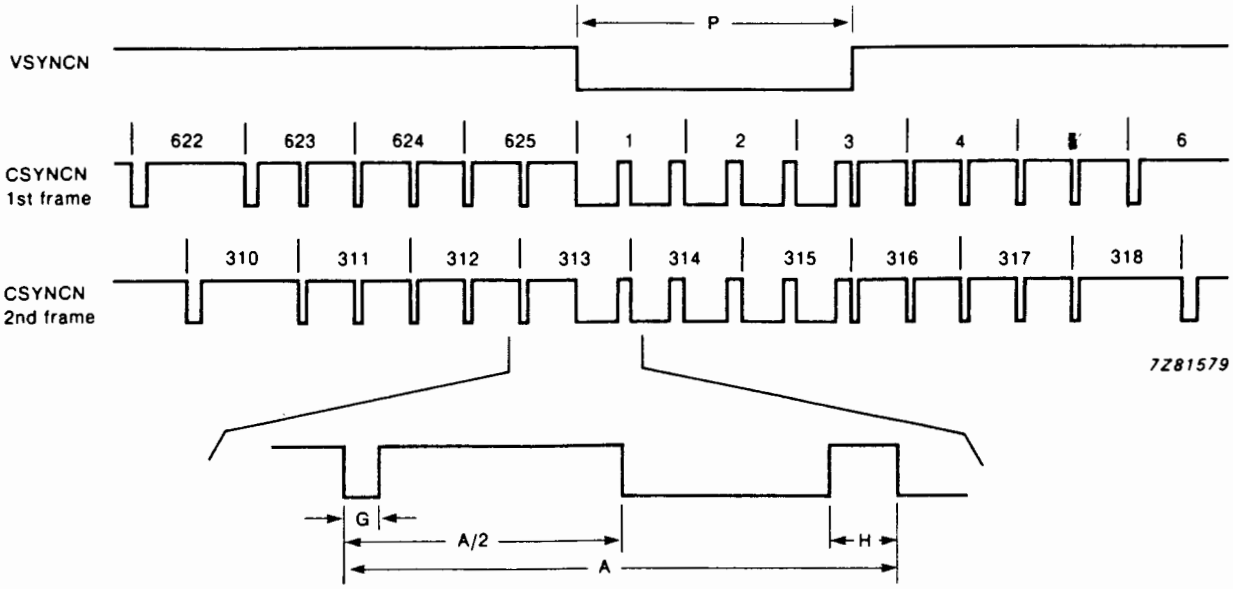


Fig. 8 CSYNCN timing in the 50 Hz interlace mode.

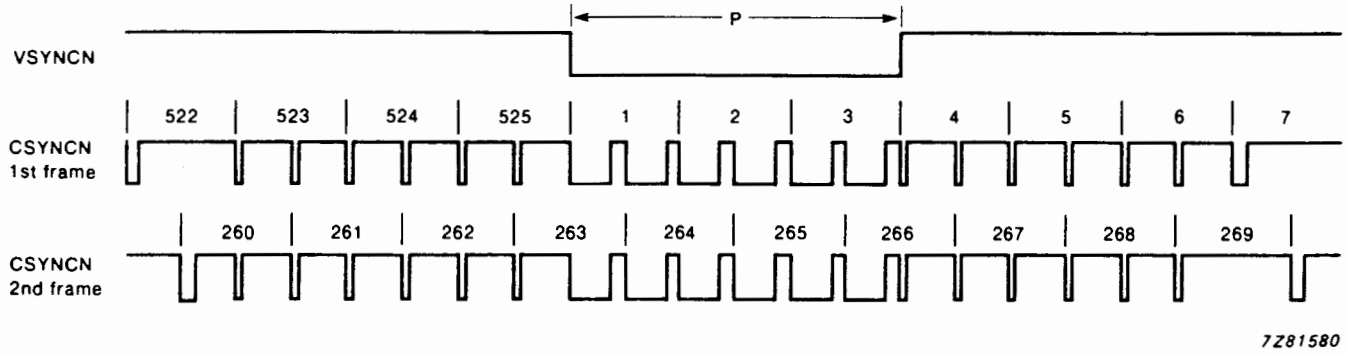


Fig. 9 CSYNCN timing in the 60 Hz interlace mode.

Frame Grabbing

When the frame grabbing bit (FG) in the DCR register is set, the SCC66470B completes the current frame before the grabbing period starts. The grabbing period consists of either one frame or two frames (interlaced mode). During this period, UWRN and LWRN are continually asserted, the DRAM can not be accessed and the MD bus is in the input mode. The CPU can poll the FG bit in the CSR register to detect the end of the grabbing period.

D. PIXEL ACCELERATOR LOGIC

The SCC66470B has on-chip pixel accelerator logic (PIXAC) to speed up the manipulation of pixel contents in memory. The PIXAC may be used in conjunction with either the CPU or the coprocessor. The ten PIXAC operations are explained in Table 11.

In addition, the PIXAC alligns source words onto destination words, masks destination pixels and magnifies or shrinks with a factor of 2 (COPY, PATCH and COLOUR). When the IPA pin is HIGH, the system bus is disconnected internally and the PIXAC is directly connected to the DRAM bus in order to speed up data transfers. The PIXAC command register (PCR) defines the implicit PIXAC register.

Table 11 PIXAC Operations

operation	description
COPY	Source pixels are copied into destination pixels.
PATCH	Source pixels other than transparent source pixels are copied into destination pixels.
EXCHANGE	Source pixels are exchanged with destination pixels.
SWAP	Source pixels other than transparent source pixels are exchanged with destination pixels.
COLOUR 1	For non-transparent source pixels, destination pixels are changed to the current foreground colour. For transparent source pixels, destination pixels are not affected.
COLOUR 2	For non-transparent source pixels, destination pixels are changed to the current foreground colour. For transparent source pixels, destination pixels are changed to the current background colour.
BCOLOUR 1	Source word bits are extended into pixels via the pixel path. For source bits that are set, destination pixels are changed to the foreground colour. For source bits that are reset, destination pixels are not affected. An index register, which is automatically incremented, points to the source nibble to be processed.
BCOLOUR 2	Source word bits are extended into pixels via the pixel path. For source bits that are set, destination pixels are changed to the foreground colour. For source bits that are reset, destination pixels are changed to the current background colour. An index register, which is automatically incremented, points to the source nibble to be processed.
COMPARE	Source pixels are compared with transparent colour. The result is stored in the most significant nibble of the B register.
COMPACT	Source pixels are compared with transparent colour. The result of each test is stored in a nibble pointed to by an index register. The index register is automatically incremented.

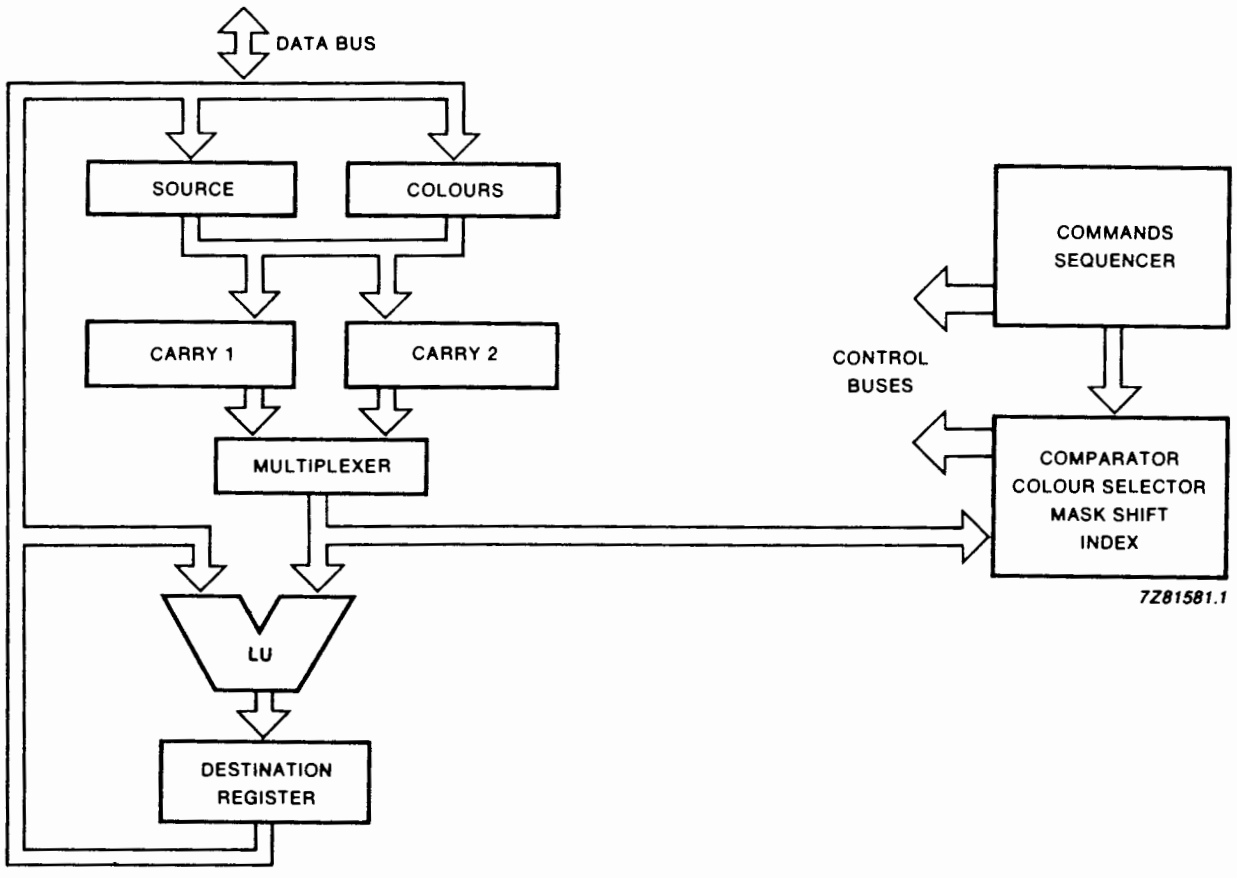


Fig. 10 PIXAC block diagram.

E. COPROCESSOR INTERFACE

The SCC66470B contains an interface which enables another CPU or coprocessor to access the DRAM, PIXAC and CSR registers. A coprocessor may be connected to the VSC via the Memory Data (MD) bus, the Memory Address (MA) bus and the Control lines. Handshake pins CYREQN, CYACKN and RASN are provided to request and acknowledge data exchange between the VSC and a coprocessor.

Interface

Three types of exchange are possible. These are:

Type A: an exchange between the coprocessor memory
Type B: an exchange between the coprocessor and the PIXAC
Type C: an exchange between memory and the PIXAC registers (controlled by the coprocessor).

An exchange takes place as follows:

1. The coprocessor asserts CYREQN.
2. On the rising edge of CYACKN, the coprocessor supplies address and control information on the MA and MD buses.
3. On the falling edge of RASN, the MA bus and CYREQN must be released. The data bus (MD) must be released for a Type C exchange or a read cycle. For a Type A exchange, a Type B exchange or a write cycle, the data bus must contain the written data.
4. For a Type A or Type B exchange, the rising edge of a second CYACKN pulse indicates that the exchange is complete and that the data bus must be released for a write cycle.

Information transfer between the coprocessor and the MA and MD buses is shown in Table 12.

A1 to A20 are the coprocessor address lines (word address). R/WNh and R/WNl are the higher and lower byte write signals for the DRAM.

SELA or SELB are asserted during a type C exchange and correspond to direct addressing of the PIXAC.

Character ROM Access

Setting the CG bit in the CSR register enables a Type C exchange with ROM. The ROM must reside in memory Bank 3 and ROM addresses must be latched after the first CAS3N assertion. ROM data is output enabled by the CSCGN signal. The exchange will be complete when CSCGN becomes inactive.

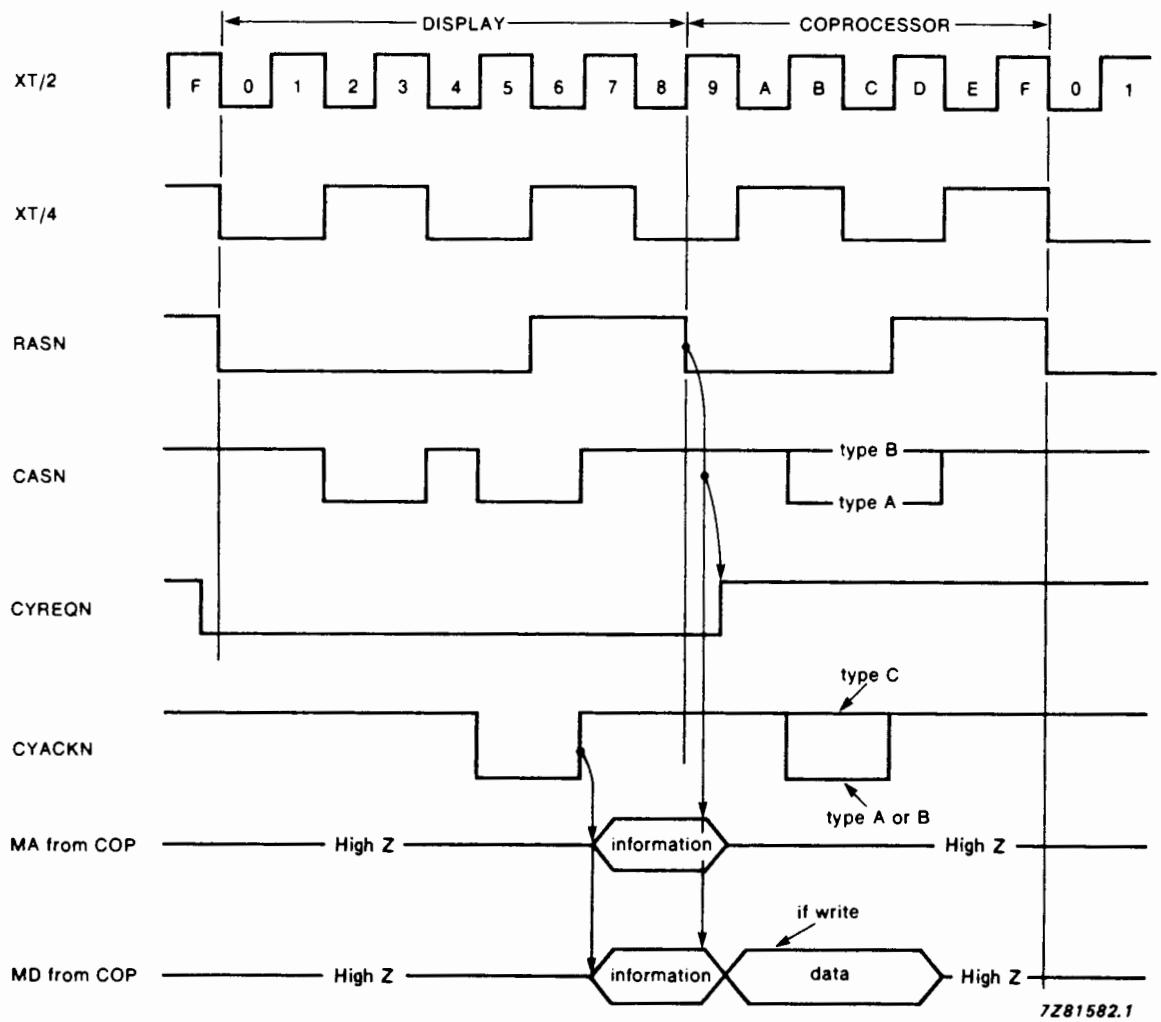


Fig. 11 Coprocessor interface in the FAST mode.

Table 12 Coprocessor data exchange

coprocessor information	256 K DRAM			64 K DRAM	
	normal and nibble	page	VRAM	normal and nibble	page
A1	MA0 R	MD0 C	MD0 C	MA0 R	MD0 C
A2	MA1 R	MA1 R	MD1 C	MA1 R	MA1 R
A3	MA2 R	MA2 R	MD2 C	MA2 R	MA2 R
A4	MA3 R	MA3 R	MD3 C	MA3 R	MA3 R
A5	MA4 R	MA4 R	MD4 C	MA4 R	MA4 R
A6	MA5 R	MA5 R	MD5 C	MA5 R	MA5 C
A7	MA6 R	MA6 R	MD6 C	MA6 R	MA6 R
A8	MA7 R	MA7 R	MD7 C	MA7 R	MA7 R
A9	MA8 R	MA8 R	MD8 C	MA8 C	MA8 C
A10	MD0 C	MA0 R	MA0 R	MD0 C	MA0 R
A11	MD1 C	MD1 C	MA1 R	MD1 C	MD1 C
A12	MD2 C	MD2 C	MA2 R	MD2 C	MD2 C
A13	MD3 C	MD3 C	MA3 R	MD3 C	MD3 C
A14	MD4 C	MD4 C	MA4 R	MD4 C	MD4 C
A15	MD5 C	MD5 C	MA5 R	MD5 C	MD5 C
A16	MD6 C	MD6 C	MA6 R	MD6 C	MD6 C
A17	MD7 C	MD7 C	MA7 R	MD7 CAS	MD7 CAS
A18	MD8 C	MD8 C	MA8 R	MD8 CAS	MD8 CAS
A19	MD9 CAS	MD9 CAS	MD9 CAS	not used	
A20	MD10 CAS	MD10 CAS	MD10 CAS	not used	
SELA	MD12	MD12	MD12	MD12	MD12
SELB	MD13	MD13	MD13	MD13	MD13
R/WNI	MD14	MD14	MD14	MD14	MD14
R/WNh	MD15	MD15	MD15	MD15	MD15

REGISTER DESCRIPTION

The SCC66470B registers are described in Table 13.

Table 13 VSC registers

register name	address (Hex)	R/W	bit number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR*	1FFFE0	W	X	X	X	X	X	X	X	X	DM1	DM2	TD	CG	DD	ED	0	BE
CSR*	1FFFE0	R	X	X	X	X	X	X	X	X	DA	FG	X	X	X	IT2	IT1	BE
DCR	1FFFE2	W	DE	CF1	CF2	FD	SM	SS	LS	CM	FG	DF	IC	DC	dt	dt	dt	dt
VSR	1FFFE4	W	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt
BCR*	1FFFE6	W	X	X	X	X	X	X	X	X	dt	dt	dt	dt	dt	dt	dt	dt
SWM	1FFFEC	W	dt	dt	dt	dt	dt	dt	dt	dt	X	X	X	X	X	X	X	X
STM*	1FFFEE	W	X	X	X	X	X	X	X	X	dt	dt	dt	dt	dt	dt	dt	dt
A	1FFFF0	W	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt
B	1FFFF2	R/W	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt	dt
PCR	1FFFF4	W	4N	COL	ENC	CPY	CMP	RTL	SHK	ZOM	dt	dt	dt	dt	INV	BIT	TT	0
MASK*	1FFFF6	W	X	X	X	X	X	X	X	X	X	X	X	X	dt	dt	dt	dt
SHIFT*	1FFFF8	W	X	X	X	X	X	X	dt	dt	X	X	X	X	X	X	X	X
INDEX*	1FFFFA	W	X	X	X	X	X	X	X	X	X	X	X	X	X	X	dt	dt
FC*	1FFFFC	W	dt	dt	dt	dt	dt	dt	dt	dt	X	X	X	X	X	X	X	X
BC*	1FFFFC	W	X	X	X	X	X	X	X	X	dt	dt	dt	dt	dt	dt	dt	dt
TC*	1FFFFE	W	dt	dt	dt	dt	dt	dt	dt	dt	X	X	X	X	X	X	X	X

Where:

dt = data.
X = don't care
* = byte addressable.

SYSTEM AND DISPLAY ORIENTED REGISTERS

The Control and Status Register, CSR

The CSR register controls the system related functions of the SCC66470B. When written to, it functions as a CONTROL register. When read, its acts as a STATUS register. It is reset to zero during the initialization sequence.

symbol	function
	Control Register (write operations)
DM1 DM2	DRAM access mode control bits. Four configurations may be selected as follows: DM1 | DM2 | Timing Speed | DRAM Mode 0 | 0 | SLOW Mode | Normal Mode 0 | 1 | FAST Mode | Page Mode 1 | 0 | FAST Mode | Nibble Mode 1 | 1 | SLOW Mode | Dual-Port VRAM Mode
TD	DRAM type (0 to 64 K devices or 1 to 256 K devices)
CG	Enables the character generator mode when set. When this mode is enabled, the timing of the CAS3N and CSCGN signals becomes ROM compatible for a coprocessor access.
DD	ROM data acknowledge delay. When DD is set, the DTACK delay changes from approximately 16 clock periods to 8 clock periods.
ED	Early DTACK. When ED is set, data will be acknowledged (DTACK asserted) when the data becomes available on the system bus and an early DTACK will be generated 2 slots (66 ns with a 30 MHz oscillator) before the data is valid.
BE	Bus error enable. When BE is set, the watchdog timer is activated and a BERR is generated.
	Status register (read operations)
DA	Vertical display active. The DA bit is set when the display controller is fetching information from the video memory. It is not affected by a horizontal retrace.
FG	This bit is set when frame grabbing is enabled by setting the FG bit in the DCR register. It is reset at the end of the frame grabbing period which has a duration of either one frame or two frames (interlaced mode).
IT1	IT1 can be set by the DCA mechanism to generate an interrupt request to the CPU. The INTN pin will go LOW simultaneously. The IT1 bit is automatically reset and the INTN output is automatically deactivated when the CPU reads the status register.
IT2	IT2 can be set by clearing bits 11 to 14 of the PIXAC command register (PCR). This action tells the CPU that the PIXAC is free and generates an interrupt request by asserting the INTN output. INTN is automatically reset when the CPU reads the status register or when one or more of the four bits in the PCR register (bits 11 to 14) is set to logic 1.
BE	This bit is set when a BUS ERROR condition has been generated by the watchdog timer. BE is automatically reset when the CPU reads the status register.

The Display Command Register, DCR

The Display Command Register (DCR) contains the four most significant bits of the Video start address and the display control bits. The 12 bits are reset to zero during the reset sequence.

<table>
<tr><th>symbol</th><th>function</th></tr>
<tr><td>DE</td><td>When set, the display enable bit enables the display controller.</td></tr>
<tr><td>CF1
CF2</td><td>These bits must be loaded with a number which corresponds to the oscillator in use as follows:
<table>
<tr><th>CF1</th><th>CF2</th><th>oscillator frequency</th></tr>
<tr><td>0</td><td>0</td><td>19.6608 MHz or 20 MHz</td></tr>
<tr><td>0</td><td>1</td><td>24 MHz</td></tr>
<tr><td>1</td><td>0</td><td>28.5 MHz</td></tr>
<tr><td>1</td><td>1</td><td>30 MHz</td></tr>
</table></td></tr>
<tr><td>FD</td><td>Frame duration control. When FD is set, the scan frequency is 60 Hz and when FD is reset, the scan frequency is 50 Hz.</td></tr>
<tr><td>SM
DF</td><td>These two bits select the scan mode. Four scan modes may be selected as follows:
<table>
<tr><th>SM</th><th>DF</th><th>scan mode</th></tr>
<tr><td>0</td><td>0</td><td>Non-interlaced</td></tr>
<tr><td>0</td><td>1</td><td>Double frequency (not possible with 20 MHz oscillator)</td></tr>
<tr><td>1</td><td>0</td><td>Interlaced</td></tr>
<tr><td>1</td><td>1</td><td>Interlaced field repeat</td></tr>
</table>
• Double frequency mode: the horizontal frequency is doubled and the vertical frequency is not affected. In this mode, horizontal resolution is halved and the vertical resolution is twice that of the non-interlaced mode.
• Interlaced mode: two interleaved frames (one odd, one even) are displayed. The VSC automatically jumps from line n to line n + 2 in the same frame. This is not possible in the physical screen.
• Interlaced field repeat mode: two identical interleaved frames are displayed.</td></tr>
<tr><td>SS</td><td>Screen Size control. When SS is set, a full screen display is generated. When SS is reset, a display with borders is generated.</td></tr>
<tr><td>LS</td><td>Logical Screen select. LS selects either a Logical Screen (LS = 1) or a Physical Screen (LS = 0). A Logical Screen requires 512 bytes per video line regardless of the status of CF1 and CF2.</td></tr>
<tr><td>CM</td><td>Colour Mode select. When CM is set, the 4 bits per pixel mode is selected. When CM is reset, the 8 bits per pixel mode is selected.</td></tr>
<tr><td>FG</td><td>Frame Grabbing enable. Setting FG provokes frame grabbing during the next frame (or during the next 2 frames in the interlace mode). It is automatically reset after the grabbing operation. FG may be read from the CSR status register.</td></tr>
<tr><td>IC
DC</td><td>IC and DC select various mechanisms as follows:
<table>
<tr><th>IC</th><th>DC</th><th>mechanism</th></tr>
<tr><td>0</td><td>0</td><td>ICA and DCA inactive</td></tr>
<tr><td>0</td><td>1</td><td>ICA active, Reduced DCA Mode (DCA size = 16 bytes)</td></tr>
<tr><td>1</td><td>0</td><td>ICA active, DCA inactive</td></tr>
<tr><td>1</td><td>1</td><td>ICA active, DCA active (DCA size = 64 bytes)</td></tr>
</table></td></tr>
<tr><td>A16 to A19</td><td>Four most significant bits of the Video Start Address. These four bits are used in conjunction with the VSR register.</td></tr>
</table>

The Video Start Register, VSR

The 16 bit VSR register and bits 0 to 3 of the DCR register constitute the 20 bit Video Start Register. The address must be Long Word aligned but a 2 bit offset can be specified for rolling purposes in logical and reduced screen modes. The VSR register is used to point to the first line of the screen or subscreen. The reload VSR instruction in ICA/DCA is equivalent to indirect addressing. The VSR register can be used as an ICA/DCA pointer.

The Border Colour Register, BCR

The 8 bit BCR register contains the Border colour. In the 4 bits per pixel mode, only bits 4 to 7 are significant.

PIXAC REGISTERS

The PIXAC logic contains registers necessary for data manipulation between source and destination registers. Only the destination register can be read.

Source Register A

Register A is a 16 bit data register which must be loaded with the source word to be processed. During an EXCHANGE operation, register A contains the source word and destination word alternatively. Writing to register A causes certain pixac functions to be triggered.

Table 14 PCR Bit Register

bit number	symbol	description
15	4N	When this bit is set, there are 8 bits per pixel. When 4N is reset, there are 4 bits per pixel.
14	COL	When set, the COLOUR and BCOLOUR functions are enabled.
13	EXC	When set, the EXCHANGE and SWAP functions are enabled.
12	CPY	When set, the COPY and PATCH functions are enabled.
11	CMP	When set, the COMPARE and COMPACT functions are enabled.
10	RTL	RTL defines the data manipulation direction in order to avoid problems when the source and destination overlap. Depending on the state of RTL, the effective carry register is either carry 1 (CY1) or carry 2 (CY2). When RTL is set, manipulation is from right to left and when RTL is reset, manipulation is from left to right.
9	SHK	When set, the source size is reduced by a factor of 2. During COPY and PATCH operations, the first pixel and the third pixel in a word are manipulated. During BCOLOUR operations, the first and third bits are manipulated. SHK does not affect any other function.
8	ZOM	When set, the source size is zoomed by a factor of 2. During COPY and PATCH operations, each source pixel is duplicated. During BCOLOUR operations, each source bit is duplicated. ZOM does not affect any other function.
7 to 4	LGF	These four bits contain the code for one of 16 possible functions performed between the source word and the expected result from the pixel path (see Logical Functions).
3	INV	When set, the transparency state of source pixels or source bits is inverted. For COLOUR1 and BCOLOUR1, the destination pixels which are overwritten change to the current background colour instead of the foreground colour.
2	BIT	BIT affects the COPY, COLOUR, EXCHANGE and COMPARE operations as follows: COPY: BIT = 0 enables COPY type B; BIT = 1 enables COPY type A COLOUR: BIT = 0 enables COLOUR; BIT = 1 enables BCOLOUR EXCHANGE: BIT = 0 normal exchange sequence; A is first loaded with the source word and then the destination word; BIT = 1 inverted exchange sequence; A is first loaded with the destination word and then the source word COMPARE: BIT = 0 enables COMPARE; BIT = 1 enables COMPACT
1	TT	When TT is set, the PIXAC logic performs a transparency test between the source pixels and the transparent colour TC. When the test is positive, the respective destination pixels are not overwritten. TT is used for enabling the PATCH, SWAP, COLOUR1 and BCOLOUR1 functions.

Destination Register B

Register B is a 16 bit data register which must be loaded with the destination word before the pixels are processed. At the end of the process, register B holds the result. Writing to register B causes certain pixac functions to be triggered.

Pixac Command Register PCR

This 16 bit register specifies the required operation and must be loaded prior to any data manipulation. Table 15 describes the PCR register.

Logical functions

The pixac logic can perform operations between the result (R) of the pixel data path and the contents (D) of register B. The result (D') is stored in register B. The Logical Function bits (bits 4 to 7 in the PCR register) define the logical operation as shown in Table 16.

Mask Register

This 4 bit register is used during pixel manipulation to mask nibbles within the destination word. When reset to zero, the corresponding nibble is not affected by the pixac logic.

Shift Register

This 2 bit register specifies the shift to be performed during source alignment (see Table 17).

Table 16 Logical functions

LGF bit number 3 2 1 0	function
0 0 0 0	D' = R
0 0 0 1	D' = NOT R
0 0 1 0	D' = 0
0 0 1 1	D' = 1
0 1 0 0	D' = NOT (D XOR R)
0 1 0 1	D' = D XOR R
0 1 1 0	D' = D AND R
0 1 1 1	D' = NOT D AND R
1 0 0 0	D' = NOT D AND NOT R
1 0 0 1	D' = D AND NOT R
1 0 1 0	D' = NOT D OR R
1 0 1 1	D' = D OR R
1 1 0 0	D' = D OR NOT R
1 1 0 1	D' = NOT D OR NOT R
1 1 1 0	D' = D
1 1 1 1	D' = NOT D

Table 17 Shift operation

source	s1	s2	s3	s4
carry	cy1	cy2	cy3	cy4
result with shift = 0	s1	s2	s3	s4
result with shift = 1	cy4	s1	s2	s3

Note: When the pixac is in the 8 bits per pixel mode (4N = 1), the shift values are 0 and 2.

Table 15 The Pixac Command Register

		PCR bit number and symbol												
operation	TRIG (see note)	15 4N	14 COL	13 EXC	12 CPY	11 CMP	10 RTL	9 SHK	8 ZOM	7 to 4 LGF	3 INV	2 BIT	1 TT	0 X
COPY, type A	A	n	0	0	1	0	n	n	0	nnn	X	1	0	0
COPY, type B	B	n	0	0	1	0	n	0	n	nnn	X	0	0	0
PATCH, type A	A	n	0	0	1	0	n	n	0	nnn	n	1	1	0
PATCH, type B	B	n	0	0	1	0	n	0	n	nnn	n	0	1	0
EXCHANGE	A	n	0	1	0	0	0	0	0	nnn	X	n	0	0
SWAP	A	n	0	1	0	0	0	0	0	nnn	n	n	1	0
COLOUR1	B	n	1	0	0	0	n	0	0	nnn	n	0	1	0
COLOUR2	B	n	1	0	0	0	n	0	0	nnn	X	0	0	0
BCOLOUR1	B	n	1	0	0	0	0	n	n	nnn	n	1	1	0
BCOLOUR 2	B	n	1	0	0	0	0	n	n	nnn	X	1	0	0
COMPARE	A	n	0	0	0	1	0	0	0	nnn	n	0	0	0
COMPACT	A	n	0	0	0	1	0	0	0	nnn	n	1	0	0

Note:

TRIG operations can be triggered by writing to either register A or register B.
The name of the relevant register (A or B) is indicated.
X = don't care;
n = 0 or 1.

Index Register

For BCOLOUR operations, this 2 bit pointer determines which nibble in the source word is to be used. For COMPACT operations, the index register determines which nibble will hold the result. In all cases (4 or 8 bits per pixel, ZOOM, SHRINK etc.), it is automatically incremented after the pixac operation.

Foreground Colour Register FC

This 8 bit register contains the foreground colour which is used for COLOUR and BCOLOUR operations. In the 4 bits per pixel mode, both nibbles are alternately displayed.

Background Colour Register BC

This 8 bit register contains the background colour which is used for COLOUR and BCOLOUR operations. In the 4 bits per pixel mode, both nibbles are alternately displayed.

Transparent Colour Register TC

This 8 bit register contains the transparent colour. In the 4 bits per pixel mode, both nibbles are alternately tested.

Selective Write Mask Register SWM

This 8 bit register contains the 'selective write mask'. This feature enables each byte of the B register to be simultaneously masked by the contents of the SWM register. This allows manipulation of groups of bits of any length up to 8 bits.

Selective Test Mask Register STM

This 8 bit register is used as the 'selective test mask' register for COLOUR functions. For the other functions, it is used internally and the BC register becomes the effective STM register. The 'selective test mask' feature allows the transparency test on bits indicated by the STM register to be disabled. This allows many transparent colours for a given operation and manipulation of groups of bits of any length up to 8 bits.

ELECTRICAL SPECIFICATIONS

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+ 7.0	V
Input voltage	V_I	−0.3	V_{DD} + 0.3	V
Output voltage	V_O	−0.3	V_{DD} + 0.3	V
Output current	I_O	–	± 20	mA
Power dissipation	P_{tot}	–	500	mW
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

DC CHARACTERISTICS

V_{DD} = 5 V (± 5%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C; all voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	conditions	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	4.5	5.0	5.5	V
Static supply current	I_{DDS}	–	–	–	250	μA
Operating supply current	I_{DDO}	XTAL = 30 MHz	–	–	65	mA
TTL input voltage HIGH A1 to A20, UDSN, LDSN. CSN, R/WN	V_{IH}	V_{DD} = 5 V	2.2	–	–	V
TTL input voltage LOW MSN, CASnN, MA0 to MA8, MD0 to MD15, HSYNCN, VSYNCN, CSYNCN, CYREQN, D0 to D15	V_{IL}	V_{DD} = 5 V	–	–	0.8	V
Input leakage current	I_{LI}	–	−10	–	10	μA
Output voltage HIGH D0 to D15, MA0 to MA15, DA, CSCGN, DTN, PCLK, WRPN	V_{OH}	I_O = 4 mA	V_{DD}−0.8	–	–	V
Output voltage HIGH CSYNCN, HSYNCN, VSYNCN, BLANKN, CSROMN, CSION, XT/2, XT4, UWRN, LWRN, CYACKN	V_{OL}	I_O = 4 mA	–	–	0.4	V
Output voltage (RASN, CASN)	V_{OH}	I_O = 8 mA	V_{DD}−0.8	–	–	V
	V_{OL}	I_O = 8 mA	–	–	0.4	V
Output leakage current	I_{LO}	–	−10	–	10	μA
Input capacitance	C_I	V_{DD} = V_I = 0	–	–	10	pF
Output capacitance	C_O	V_{DD} = V_I = 0	–	–	15	pF
Input/output capacitance	$C_{I/O}$	V_{DD} = V_I = 0	–	–	15	pF

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{DD} = 5 V (± 5%); V_{SS} = 0 V; T_{amb} = 0 to + 70 °C; V_{IL} = 0 V; V_{IH} = 3 V; V_{OL} = V_{OH} = 1.3 V. C_L (MA0–MA8, UWRN, LWRN) = 80 pF; C_L (CAS1N–CAS4N, RASN) = 160 pF; C_L (MD0–MD15) = 75 pF; C_L (system signals) = 130 pF; C_L (XT/2, PCLK, V0–V7; WRPN, CYACKN, BLANKN, DA) = 75 pF.

parameter	symbol	20 MHz		24 MHz		27.5 MHz		30 MHz		unit
		min.	max.	min.	max.	min.	max.	min.	max.	
XT/2 clock period	1	100	100	85	85	73	73	67	67	ns
UDSN/LDSN LOW to slot set-up time	2	80	–	80	–	80	–	80	–	ns
Address to slot set-up time (read)	3	100	–	95	–	90	–	85	–	ns
CASN to data valid (read); note 1	4	–	55 + d	–	55 + d	–	55 + d	–	55 + d	ns
XT/2 to DTACKN LOW	5	–	20	–	20	–	20	–	20	ns
UDSN/LDSN HIGH to data 3-state	6	–	170	–	155	–	145	–	135	ns
UDSN/LDSN HIGH to DTACKN HIGH	7	–	45	–	45	–	45	–	45	ns
XT/2 to DTACKN 3-state	8	–	20	–	20	–	20	–	20	ns
UDSN/LDSN to RASN LOW in free-run	9	280	430	240	375	210	335	195	315	ns
UDSN/LDSN to CASN LOW in free-run	10	230	380	200	330	175	300	165	280	ns
XT/2 to RASN LOW	11	–20	5	–20	5	–20	5	–20	5	ns
XT/2 to CASN LOW	12	–20	5	–20	5	–20	5	–20	5	ns
XT/2 to UWRN/LWRN LOW	13	–15	10	–15	10	–15	10	–15	10	ns
XT/2 to MA0–MA8 valid	14	–10	30	–10	30	–10	30	–10	30	ns
Data to CASN HIGH set-up time	15	5	–	5	–	5	–	5	–	ns
Data to CASN HIGH hold time	16	15	–	15	–	15	–	15	–	ns
XT/2 to BLANKN/DA	17	–5	30	–5	30	–5	30	–5	30	ns
DA to 1st pixel or WRPN (no roll)	18	45	80	35	70	30	65	30	65	ns
RASN HIGH precharge time	19	140	–	115	–	100	–	90	–	ns
CASN HIGH precharge time	20	190	–	160	–	135	–	125	–	ns
CASN HIGH toggle precharge time	21	40	–	30	–	25	–	25	–	ns
XT/2 to RASN HIGH	22	–25	5	–25	5	–25	5	–25	5	ns
XT/2 to CASN HIGH	23	–20	10	–20	10	–20	10	–20	10	ns
PCLK LOW to pixel valid	24	0	25	0	25	0	25	0	25	ns
Pixel to PCLK HIGH set-up time; note 2	25	35	–	25	–	20	–	15	–	ns
CYREQN LOW to slot 3 set-up time	26	45	–	45	–	45	–	45	–	ns
CASN HIGH to CYACKN HIGH	27	10	30	10	30	10	30	10	30	ns
CYACKN HIGH to MA/MD valid	28	5	–	5	–	5	–	5	–	ns
MA/MD to RASN LOW set-up time	29	10	–	10	–	10	–	10	–	ns
MA/MD to RASN hold time	30	10	–	10	–	10	–	10	–	ns
CYREQN HIGH to MA valid	31	–	45	–	45	–	45	–	45	ns
MD to CYACKN HIGH hold time	32	0	–	0	–	0	–	0	–	ns

Notes:

1. d = DRAM access time for CASN.
2. 4 bits per pixel, FAST mode

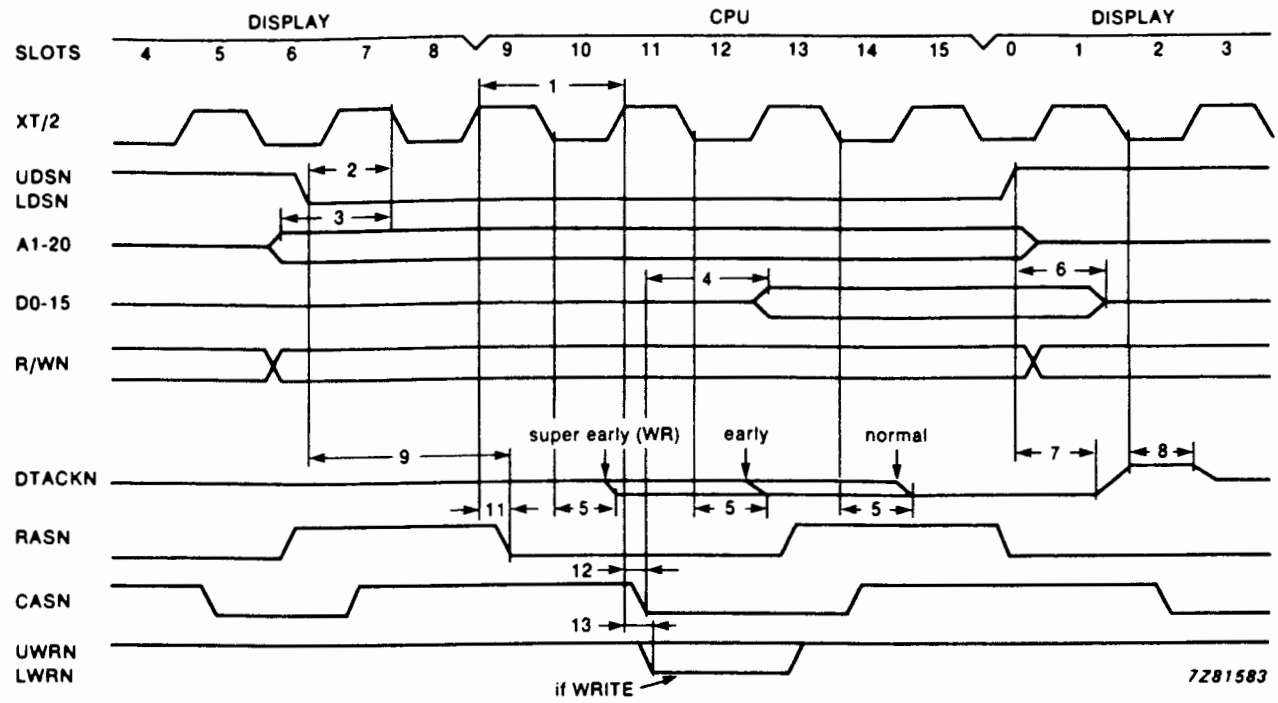


Fig. 12(a) CPU memory access in FAST mode.

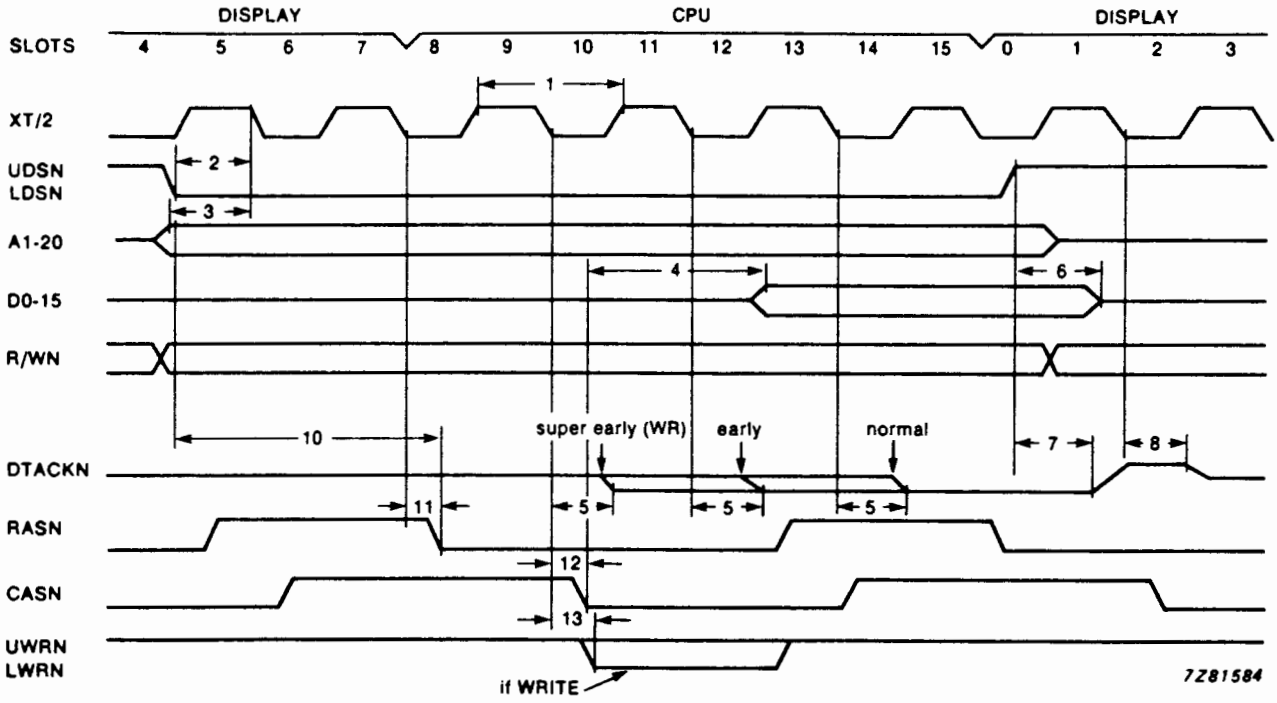


Fig. 12(b) CPU memory access in SLOW mode.

Note:

In the Dual Port VRAM mode, CPU memory access can occur during the display window.

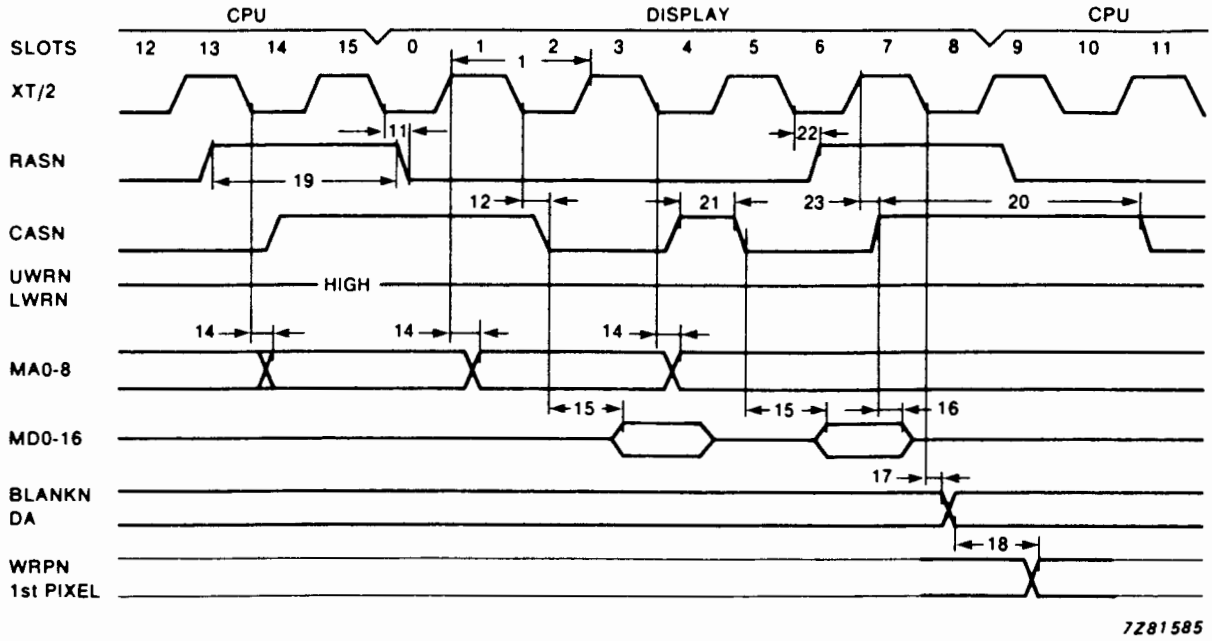


Fig. 12(c) Display cycle in FAST mode.

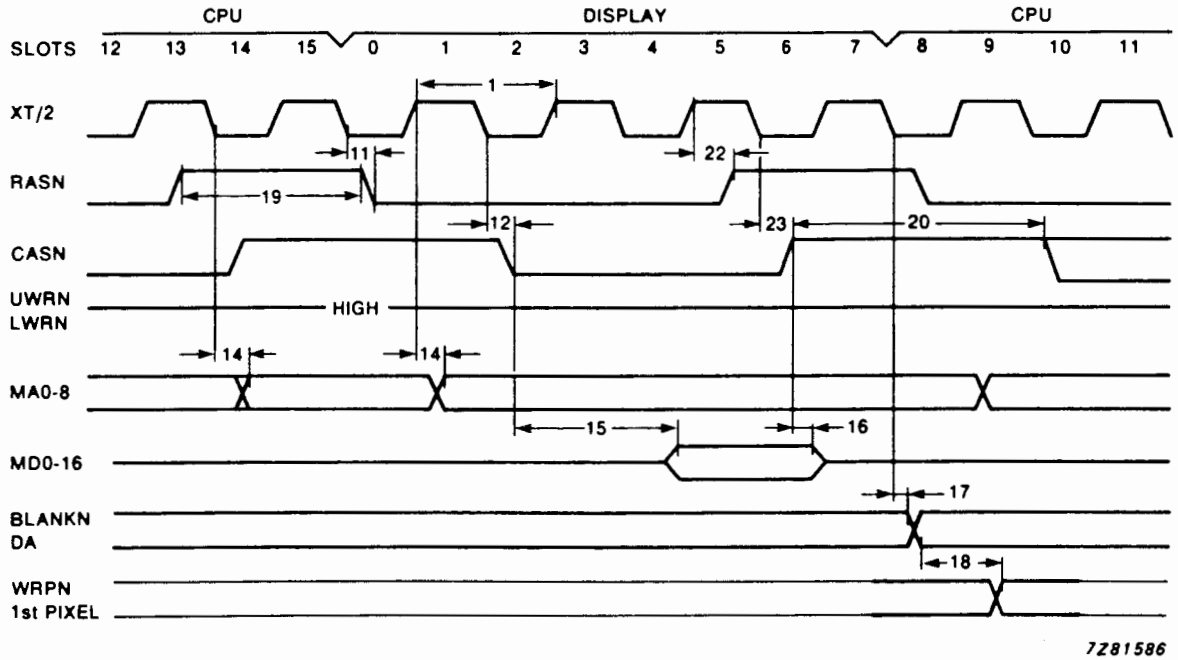


Fig. 12(d) Display cycle in NORMAL mode.

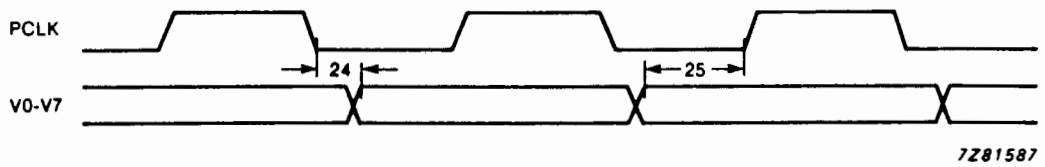


Fig. 12(e) Pixel output timing.

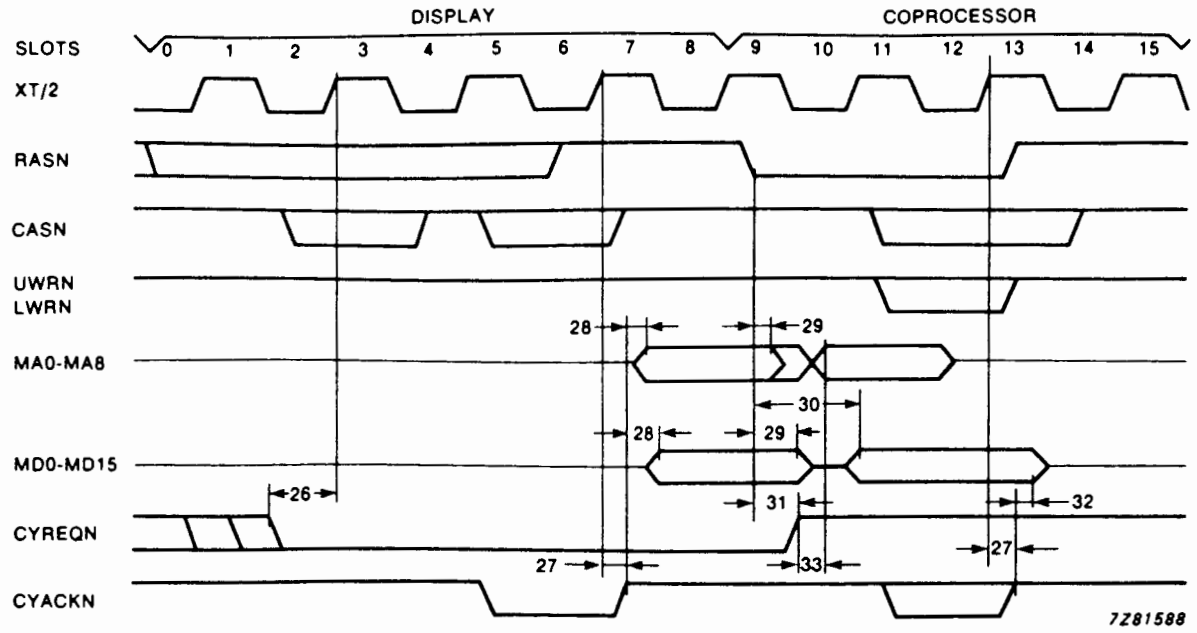


Fig. 12(f) Coprocessor, memory or register access in FAST mode.

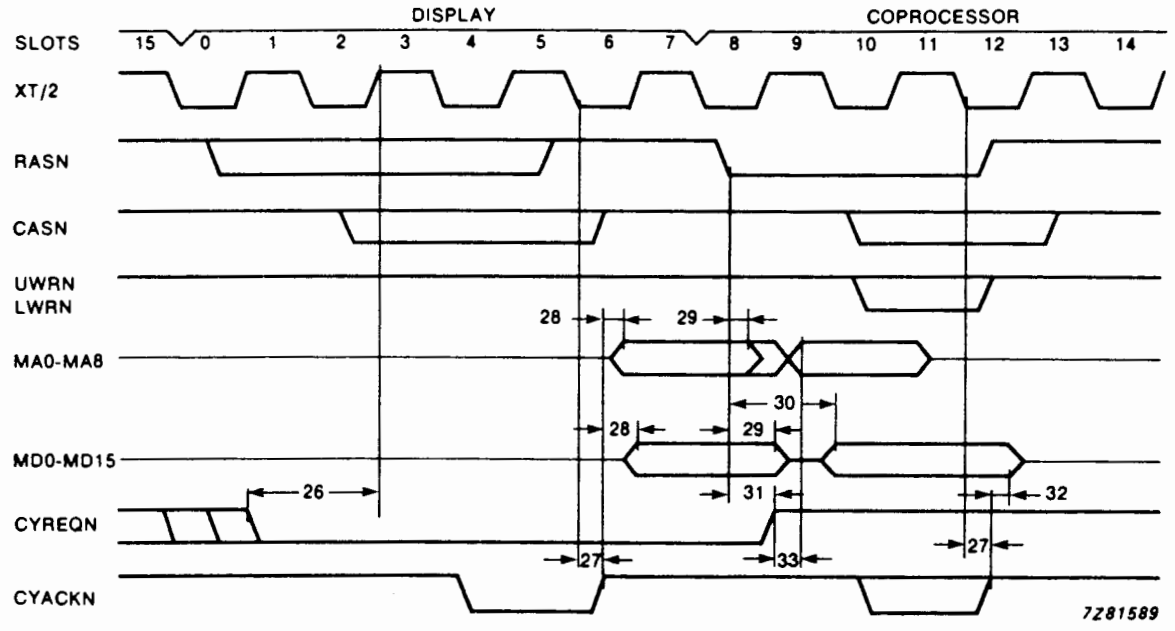


Fig. 12(g) Coprocessor, memory or register access in SLOW mode.

CLOCK CIRCUITRY

Figs 13 and 14 show how the SCC66470B clock may be derived from a crystal oscillator and from an external source.

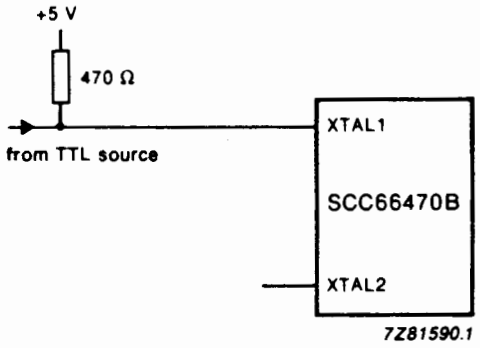


Fig. 13 Driving the SCC66470B from an external source.

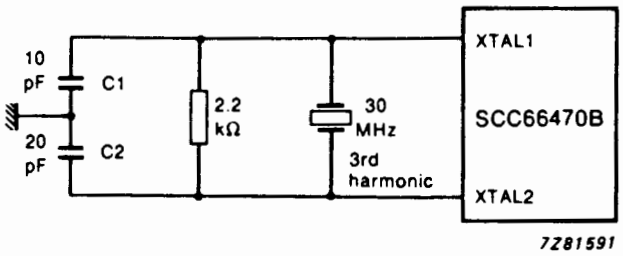
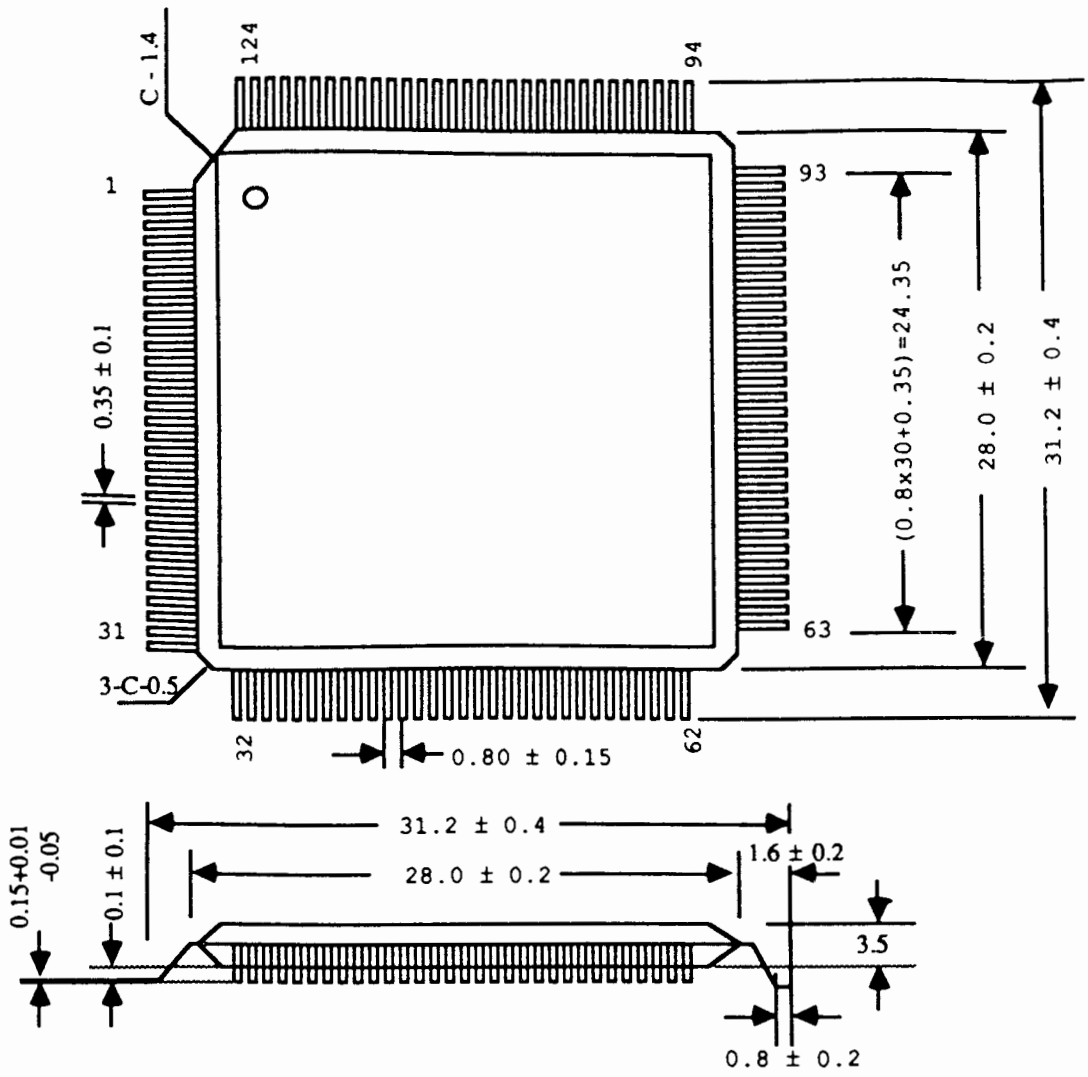


Fig. 14 Driving the SCC66470B with a crystal oscillator.

DEVELOPMENT DATA

124-LEAD QUAD FLAT-PACK; PLASTIC



PACKAGE (TOP VIEW).

Dimensions in mm

SOLDERING PLASTIC QUAD FLAT-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.