FOCUS data terminals

DESIGNING A COMPLETE VIDEO INTERFACE

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As the need for displaying data increases so does the need for video information systems which interface to microprocessors. Microprocessors and other sophisticated integrated circuits are often thought difficult to understand. This is not true. Although such elements are complex, they operate in a logical way so that understanding only requires study, explanations and guidelines. This article illustrates the design process — a process which will become increasingly common as the variety of intelligent data terminals grows — with reference to devices from RCA's 1802 microprocessor family.

The RCA 1800 series of c.m.o.s. low power microprocessor devices includes c.p.u.s, r.a.m.s, r.o.m.s, e.p.r.o.m.s, p.i.o., u.a.r.t., m.d.u., interface chips and low resolution video controllers. But as the need for displaying data increases, a high resolution video interface system — v.i.s. — has been added.

The v.i.s. consists of two c.m.o.s. l.s.i. devices — the CDP 1869 and CDP 1870. They generate all the signals needed for visualisation on the screen. In addition, a sound generator and white noise are included with volume control on the chip.

This device set interfaces directly with minimum additional hardware to an 1802 microprocessor c.p.u. but is designed as a completely independent I/O (input/output device). No refresh signals are needed that might stop the processor from synchronisation during display time. A 'predisplay' signal warns the c.p.u. one display line before refresh starts, blocking further access to v.i.s. memories until complete frame display is finished.

Internal multiplexers allow access to the v.i.s. memories for changes to character memory — dot and colour information — or page memory with character allocation on the screen. During display time, the processor is completely free for other I/O or computing.

Versatility

The v.i.s. therefore has a wide range of capabilities. Program resolution can be 40 characters in 24 rows or 20 characters in 12 rows. Character size depends on the display sytem — six dots wide by eight dots high for NTSC, 6 × 9 for PAL.

Up to 256 characters are possible with character definition in r.a.m., r.o.m. or even mixed. Eight character colours and eight background colours can be generated. Hardware scrolling is also provided.

Sound generation is possible over eight octaves with 128 frequencies in each, and there are eight noise generation ranges. Sound and noise volume control is in 16 steps each.

Chroma and luminance generation is carried out on chip and a clock signal is provided for the c.p.u. All features are under software control.

Two systems of memory are possible. In the full bit mapping approach, each memory bit represents a pixel or dot on the screen. This type is ideal for displaying curves and pictures but needs a large amount of memory. Typically, a display of 40 characters per line and 24 rows with a character size of 6 × 8 in bit map would be represented by six bits per character line times eight character lines times 40 × 24 or 960 times six times eight. This makes 45kbit built by a memory of 8kbit and six bits wide.

A second choice is to divide the screen into a surface of characters. For example, a definition of 24 rows times 40 characters would give the same resolution. The character positions on the screen would be addressed by a page memory 960 bytes long to define each of the 40 times 24 character positions.

In the character display system it is necessary to define how many different characters are possible on the screen. Eight bits are required for a maximum of 256 characters. So the 960-location-long page memory has to be eight bits wide to define which character is where. Each character is 6 × 8 bits. That means that 256 characters need 256 times 48 or 12kbits (1½kbytes). So while 1kbyte is needed for the page memory, character memory needs a further 2kbytes. (Memory is normally available in multiples of 1kbyte.)

Comparing bit maps and character maps for the same display, the former needs 8kbytes while the latter requires only 3kbytes. This comparison looks even better for a system that needs less than 256 characters: for 128 characters only 2kbytes would be required for example.

Design goals

The v.i.s. system was developed after examination of both methods. Several design goals were set, leading automatically to the approach chosen:

1) *full c.m.o.s. operation* — simplifying battery operation due to low power consumption and wide power supply range;
2) *minimum component count* — optimising the package count in the complete system, not just the video generation section;
3) *minimum memory* — leading automatically to the character mapping method as the bit map approach needs a large amount of memory (however at least some of the bit map advantages were to be retained);
4) *completely independent I/O* — avoiding c.p.u. involvement apart from changing memories or updating internal registers so that it does not have to be stopped during display and thus can be used for other tasks all the time;
5) *maximum r.f. resolution* — avoiding restrictions on high resolution displays;
6) *programmable resolution* — allowing adaptation to use such as educational display using lower resolution with greater distances between screen and observer;
7) *graphics and motion capability* — enabling animated display and semigraphic pictures;
8) *external synchronisation* — making it possible to overlay the video signals of television and v.i.s. to allow display of time and channel or received text information for example;
9) *colour* — supplying an essential facility in many applications for different colours or at least varying shades of grey for both PAL and NTSC systems as well as direct colour information in RGB (red green blue); and
10) *audio generation* — supplying programmable sound for many applications, particularly in the games area where this is required or in industrial applications for different alarms or audio prompts in terminal uses.

Two chips needed

A two-chip solution was found necessary to include most of the external hardware required, such as multiplexers and colour generators. The CDP 1869 solves address manipulation, whilst the CDP 1870 deals with video signal generation. An alternative version of the latter — the CDP 1876 — provides RGB output instead of chrominance and luminance.

Let's look first at the CDP 1869 address generation and audio chip. The 1802 microprocessor has an eight-bit multiplexed address bus and generates two timing pulses TPA and TPB to define the presence of the high and low address byte respectively. So the 1869 provides an eight-bit latch on chip to keep the high byte and implements an internal 16-bit address bus.

The control circuit recognises special instructions to set resolution, sound and noise, change memory addressing and character scanning, and provide control signals for memory and data bus buffer. These instructions are chosen by three I/O selections from the 1802; it also generates a decode signal for the 1870.

An address multiplexer decides which information goes to the address lines of the page memory. During the display time, it selects the character positions on the screen, PMA 0 to 9, and scans the character lines CMA 0 to 2. During the non-display time, the c.p.u. memory bus is connected directly to the page memory and it appears as an extension on the c.p.u. memory, fixed at F800 to FFFF. Because only 960 bytes of this memory are used — maximum 40 × 24 — in a 1k byte system, 64 bytes are free for stack or other purposes.

The address counter either defines the posi-

continued on page 71

FOCUS data terminals

continued from page 67

tions on the screen, or is used for character r.a.m. loading during non-display time.

The home address register defines the leftmost character of the first line on the screen. If it is set to 0000, the display shows an unshifted image of the page memory contents. Loaded with multiples of 40, it allows line-by-line scrolling. In low resolution mode (20 × 12) it would allow the display of four different pages on the screen.

The sound generator is designed as a three-bit prescaler and a seven-bit down scaler, loaded via a command byte from the output signal and automatically loaded with the same byte again. Resolution is three octaves, with 128 different frequencies within each octave.

Eight ranges of white noise are also provided. The result is an explosion type sound effect, useful in TV game systems. A four bit R-2R ladder network with a latch is provided to define the amplitude of the noise signal.

Video signal

Video signal generation takes place in the CDP 1870. Its control section provides signals for the data bus multiplexer to allow character memory/access from the CPU, latch signals for the control instruction and special signals to synchronise both 1869 and 1870. One input is used to switch internal logic from PAL to NTSC standards.

The data bus multiplexer is needed for character memory access if it is in r.a.m. It has an eight-bit wide input. Six bits, CDB 0 to 5, are used for character dot information. A character line is six dots long.

The next two bits — CCBO and CCBI — are used for character colour bit information. Four colours out of eight are defined per character line. The PCB input line provides the page colour bit and expands colour capabilities to eight. It is normally connected to the page memory.

If character memory is in r.a.m., it has to be initialised after power on. With this multiplexer, the character memory is switched to the c.p.u. during non-display time.

The dot oscillator provides the clock for the timing generator. Here nearly all the signals for synchronisation are generated. A special 'predisplay' signal tells the c.p.u. that one display line later, the multiplexers are switched and a refresh cycle starts.

Connected to the interrupt signal, it can decide between updating the v.i.s. and working on other parts of the program. In this way, the c.p.u. does not waste time waiting for the end of the display refresh.

Some other signals are needed to synchronise the two chips, for example increment page memory counting. The dot frequency is about 5·6MHz. This signal is divided by two and may be used as clock frequency in the c.p.u. Vertical and horizontal timing appears on Compsync.

The parallel-to-serial shift register latches one line of a character and shifts it out to the luminance and chrominance logic. Here the dot information is combined with the colour information of the character.

There are two bond options for the CDP 1870. For a terminal, it would be useless to have the complete colour video signal and separate afterwards. In this case, the CDP 1876 should be used. Colour luminance and chrominance are then replaced by red, green and blue.

To understand the various actions better, consider the complete system. This can be used as a terminal. It uses a CDP 1802 as a processor with separate r.o.m. and r.a.m.

The CDP 1869 creates sound and noise through an amplifier and addresses the page memory with PMA 0 to 9 — character position on the screen. It scans the lines of the character memory with CMA 0 to 2 and generates some signals for buffer or r.a.m. selection. Synchronisation signals come from the CDP 1870.

Programming

The v.i.s. devices are programmed using a special feature of the 1802 processor to output the information. An internal register is specified and loaded with the address of the byte to be sent.

For the 1869, connected only to the address bus, the address itself is the information — it does not use the data. The data at the memory location specified by this register is the information required by the 1870.

One instruction controls the 1870 for 20 or 40 character resolution, character colour control, character format control, display on or off and background colour definition.

Three instructions control the 1869. The first sets octave, frequency within the octave, sound amplitude and sound on and off. The second programs white noise range and amplitude, 12 or 24 line resolution, 960 or 1920 character page length, NTSC or PAL system and resolution. The third selects a fixed address for page or character memory access. A fourth instruction enables the setting of the home address register for scrolling.

A v.i.s. interpreter is available to reduce the time-consuming manipulation of software modules once design is finished. It consists of a 3kbit program with 86 different sub-routines that can be called by one-byte instructions.

The interpreter includes memory manipulation as well as colour definition, setting of sound and noise and all other control instructions. In addition, the interpreter permits interruption for the execution of machine code subroutines.

Complete interface

The v.i.s. is designed not as an interface device but as a complete interface system. Advantages include maximum flexibility with minimum demand on the c.p.u., leaving that free for the execution of other tasks. Once started, the v.i.s. can generate the display completely indpendently of the c.p.u.

Together with the c.p.u., it gives a small component count and very low power consumption with a wide temperature range. A v.i.s. board is available in RCA's Microboard range with a complete I/O system. Together with a c.p.u. board and an ASCII keyboard, it represents a complete video system with output for a colour monitor.