scheme of this microprocessor[1]. These devices also are capable of operating with a DMA controller, independently of the microprocessor. Like other serial devices for microprocessors, they are fully programmable by software, except for baud clock rate. A full description of these devices is available[2,3].

Presented here is a circuit, Figure 1, and program, Figure 2, for using a DART in polled operation for a single channel. A timer/counter CTC[4] circuit is used to generate the baud clock frequencies. The rate is detected by software and adjusted to the rate of the terminal interfaced to the DART. The standard rates from 19 200 to 50 baud can be used, including 110 baud.

The software can be expanded to work with two serial interfaces with no additional hardware. Total cost of the DART and CTC circuits is about £14, in low quantities. This compares favourably with more conventional serial interfaces for the Z80. A great deal of board 'real estate' is saved, further lowering costs. The CTC operates from the Z80 clock, so that a separate crystal for the baud generator is not required. 'Odd' clock frequencies may be accommodated by changing the CTD division ratios, although there are limits at higher baud rates.

## REFERENCES


1 'The Z80 family program interrupt structure' *Zilog* (May 1978) pp 1–31

2 'Z80-SIO product specification' *Zilog* (August 1978) pp 1–16

3 'Z-80 DART dual asynchronous receiver/transmitter product specification' *Zilog* (June 1979) pp 1–12

4 'Z80-CTC product specification' *Zilog* (March 1977) pp 1–8


# Memory considerations for a microprocessor video interface system


**G T Fogarty** describes the VIS display system


The VIS (video interface system) display system (CDP 1869 and CDP1870)[1], a minimal-device-count approach to colour-character generation, is essentially a CRT controller designed to interface to the CDP1800 series of microprocessors (CDP1802 and CDP 1804). The system relieves the CPU of generating screen refresh timing or data. Other capabilities include programmable background and character colours, white-noise and tone generator and hardware scrolling. The scheme described in this article, while requiring a few more parts, very nearly doubles the memory access-time requirement of the system and permits the use of memories approximately half as fast as those normally required with the video interface system.

## VIS SYSTEM OPERATION

The video interface system was designed with minimal chip count as a goal. A minimum I/O system requires only the CDP1869, CDP1870, page memory, character memory and two bus separator chips (Figure 1). The bus separators are required to allow the CPU to access the page memory. The character memory bus multiplexing is internal to the CDP1870.

The character generating scheme is as follows: the page memory is a sequential list of character positions on the CRT screen; its data is a pointer to the character to be displayed at that screen position. The character memory contains the actual dot pattern of all the possible characters that can be displayed. During screen refresh, the CDP1869 generates addresses to the page memory. The page memory output data, in turn, addresses the character memory,

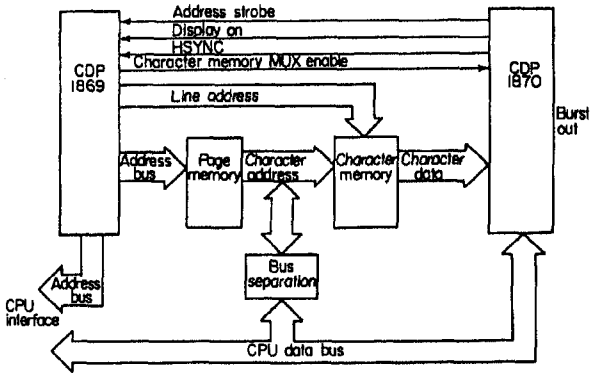


*Figure 1. A minimum I/O system*

whose data is then latched into the CDP1870 for serial output to the CRT screen.

Note that one character cycle involves two memory access times: page address to page memory; and page data (character address) to character memory. In a 40-character-per-line system, the total of these two times is about 1 μs (six dot clocks) minus the page memory address delay from the CDP1869 and the character data setup time into the CDP1870.

The timing diagram in Figure 2 shows that the signal, 'address strobe', from the CDP1870 advances the page-memory address in the CDP1869 at the trailing edge, initiating an address cycle. This signal is analogous in time to the shift-register load signal in the CDP1870. Therefore, the next 'address strobe' terminates the current access and initiates the next character access.


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## ADAPTION FOR SLOWER MEMORIES

If page and character memory were accessed in parallel, the memory speed requirement would be eased substantially. This parallel accessing can be accomplished by latching the page-memory data and keeping the page memory one character ahead of the character memory; the circuit shown in Figure 3 accomplishes this task. A TTL one-shot multivibrator was chosen for minimal delay. The multivibrator generates a pulse of approximately 200 ns starting at the trailing edge of the 'address strobe' signal, which is used to advance the address counter in the CDP1869 and to latch page-memory data. The burst signal, occurring once per horizontal sync., is used to generate the 'extra' address count. During nondisplay time, the one-shot is disabled to prevent the address counter from advancing and the latch control is held true. The latter makes the latch feed through, enabling normal character memory access. Gates A and B inhibit the last strobe in half and full resolution, which allows for proper hardware rolling or scrolling. PMA4–PMA9 are addresses 4–9 of the CDP1869 and are used for the page memory.

With this 'staggered access' circuit, page memory access starts at the trailing edge of the new strobe pulse (pulse-address-out delay) and terminates at the trailing edge of the next strobe; the total time required is approximately that to access one full character. Character memory access starts at the leading edge of the strobe signal (plus latch delay) and terminates at the data setup time requirement of the CDP1870, also approximately the time to access one full character. Since the delay through the latch is similar to the address-out delay of the CDP1870, this scheme, while it requires a few more parts, essentially doubles the memory access-time requirement of the video interface system, and permits the use with it of memories approximately half as fast as those normally required.

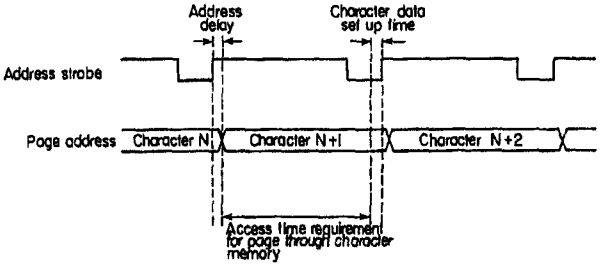


*Figure 2. Timing diagram for Figure 1*

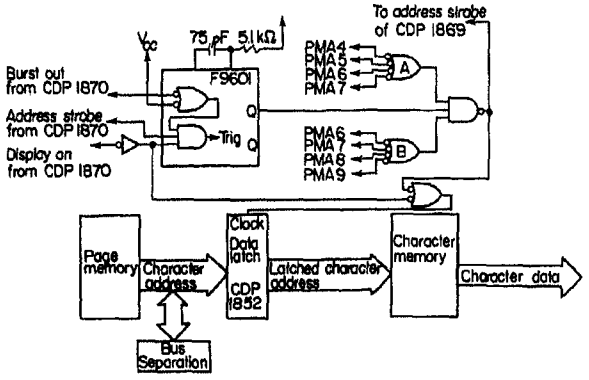


*Figure 3. Circuit used to adapt video interface system to slower memories*

## REFERENCE

1 'COS/MOS video interface system' types CDP1869 and CEP1870' *RCA Solid State Data Sheet* 1197